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USING ITERATIVE SIMULATION TO INCORPORATE LOAD-DEPENDENT LEAD TIMES IN MASTER PLANNING HEURISTICS

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ABSTRACT

In this paper, we consider heuristics for master planning in semiconductor manufacturing. While lead times are typically assumed as fixed in production planning, we use iterative simulation to take load-dependent lead times into account. An AutoSched AP simulation model of a semiconductor supply chain is used for implementing the scheme. Simulation results show that the iterative scheme converges fast and leads to less variable, more profitable production plans compared to planes obtained by the fixed lead time approach.

1 INTRODUCTION

Production planning deals with determining release schedules that try to match production output with given demand in such a way that revenue- or cost-related objective functions are optimized while capacity restrictions are taken into account. Most of the existing production planning models assume a fixed lead time as an exogenous, prescribed parameter of the planning approach (Voß and Woodruff 2006). The lead time of a product is an estimate of the cycle time in the planning algorithms. We refer to the cycle time of a product, also known as flow time, as the average time that is required to complete its processing in the production system. Production planning in semiconductor manufacturing is challenging due to the reentrant flows, the long cycle times, the high utilization of the expensive machines, the diverse product mix, and the different sources of variability.

It is well known from queueing theory that the cycle time increases nonlinearly with the utilization of the resources of the base system. However, the utilization is a result of the release schedule used. This leads to a well-known circularity in production planning. On the one hand, the planning approach determines the release schedule based on a prescribed lead time. On the other hand, the cycle time depends on the lot release schedule (Pahl et al. 2007, Missbauer and Uzsoy 2011).

Iterative simulation is one approach that tackles this circularity by iterating between a production planning model that determines production quantities based on a prescribed lead time and a discrete-event simulation model that uses these production quantities to calculate new flow time estimates (Hung and Leachman 1996, Almeder et al. 2009, Irdem et al. 2010 among others).

In this paper, we are interested in applying the iterative simulation approach to a specific multi-facility, multi-product, and multi-period master planning problem. The problem includes important features of semiconductor supply chains like reentrant process flows, outsourcing options, and multiple products with long process flows. The master planning problem and exact and heuristic approaches to efficiently solve it are discussed by the two present authors in (Ponsignon and Mönch 2012). However, a fixed lead time is assumed for all products in this paper. A one-stage supple chain consisting of four scaled-down wafer fabs is represented by a simulation model. To the best of our knowledge, iterative

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simulation is not used so far for supply chains in the semiconductor industry. We show by performing designed experiments that the iterative scheme converges for our problem.

The paper is organized as follows. The researched problem, including the master planning heuristic, is described in the next section. Related literature is also discussed. The iterative scheme is presented in Section 3. The results of computational experiments are shown and analyzed in Section 4.

2 PROBLEM

2.1 Master Planning Heuristic

We consider a master planning problem in a one-layer semiconductor manufacturing network consisting of wafer fabs as nodes, i.e., there is no flow of quantity across the nodes (see Figure 1). The problem is denoted by MPSC throughout the paper. We are interested in determining appropriate wafer quantities for the planning horizon for a set of products $P := \{1,..., p_{\max}\}$ that can be processed in $m_{\max}$ front-end (FE) facilities. The market demand is given by firm orders and supply reservations. It is assumed that inventory is possible. Unmet firm orders are carried over as backlog to the next period. The capacity limits are related to bottleneck work centers. The planning horizon considered is 26 periods.

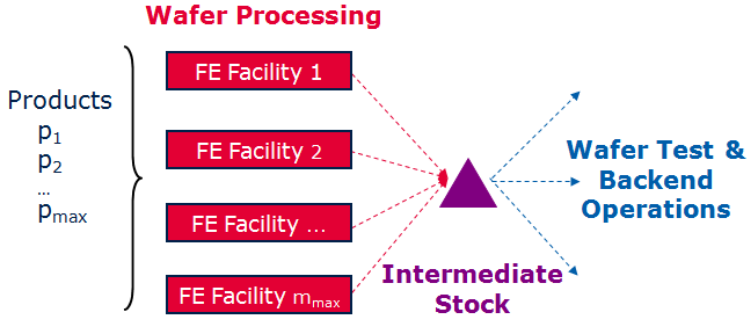

Figure 1: One-layer semiconductor manufacturing network for wafer processing.

It is assumed for MPSC that all products have a fixed lead time. The problem contains an objective function related to the difference between revenues and total costs, and it is subject to a set of constraints. The objective function strives to keep the number of unmet firm orders low and to satisfy supply reservations if capacity is sufficient, whereas the inventory level is minimized accordingly. The production can be outsourced to silicon foundries if more capacity is required. An inexpensive assignment of products to in-house facilities and silicon foundries is privileged. The production partitioning over different facilities is limited with respect to fixed production costs.

The heuristic approach researched in the present paper is a rule-based assignment procedure denoted by RA-MPSC. First, the product with the highest backlog cost or the highest revenue is selected. Then, the demand for the selected product in the current time period is allocated to the wafer fab with the most remaining capacity. When capacity is not sufficient in the actual period, the algorithm looks for available capacity in previous time periods. This leads to pre-production and stock building but it avoids backlogs. If the demand cannot be entirely assigned to a single wafer fab, an additional wafer fab with the second most remaining capacity is selected. We do not assign the demand for a the selected product in the current time period to more than two wafer fabs to minimize the production partitioning. This procedure is repeated until all products and all time periods have been considered. Note that orders are allocated with a higher priority than forecast. In addition, minimum and maximum capacity limits are strictly respected. Indeed, if the load is too low, it is increased by means of a repair loop. For more details on this heuristic, we refer to (Ponsignon and Mönch 2012).

Next we describe how the fixed lead time is represented in RA-MPSC. The index $k = 0,...,k_{max}$ is used to calculate the capacity consumption of a product. We assume that the product has a cycle time of

$k_{max}+1$ weeks and that $b_{\max}$ bottlenecks exist in a specific facility. We use product- and facility-specific capacity consumption matrices $C \in IR^{b_{\max} \times (k_{\max}+1)}$, where the elements cc_{bk} of C model the capacity consumption of one wafer when this wafer is processed on bottleneck b with $1 \le b \le b_{\max}$ and its completion period is $0 \le k \le k_{\max}$ periods ahead. When the route of a product and a lead time is given, the matrices can be determined using the flow factor that corresponds to the given lead time. Note that this approach allows to deal with reentrant process flows.

RA-MPSC determines the number of wafers x_{pmt} that have to be completed in each period t for product p and facility m. Then a release schedule $\widetilde{x}_{pmt}$ can be calculated by using a backward loading scheme and a simple lot sizing rule.

2.2 Discussion of Related Work

An iterative linear programming-simulation scheme is proposed by Hung and Leachman (1996) for production planning in wafer fabs. However, only a limited set of experiments is carried out to assess the performance of the scheme. Kim and Kim (2001) discuss another iterative approach for production planning. Irdem et al. (2010) show that only the latter approach unambiguously converges when it used for production planning in wafer fabs. A disadvantage of the iterative simulation approaches for wafer fabs is the huge computational burden that is caused by the repeated simulation runs. Almeder et al. (2009) uses iterative simulation in a supply chain context. However, the setting considered there is quite different from semiconductor manufacturing.

Another stream of production planning research with load-dependent lead times is related to clearing functions (Missbauer and Uzsoy 2011). A clearing function provided the expected aggregated output of a tool group as a function of an appropriate measure of work in progress (WIP), typically aggregated over all products. The tool group-specific clearing functions are incorporated into the linear programming formulations for production planning. The clearing functions are derived from simulation output. It is a nontrivial task to fit appropriate clearing functions for the tool groups of a wafer fab. Kacar et al. (2012) compare the performance of clearing function- and iterative simulation-based linear programming formulations for production planning in a scaled-down wafer fab. It turns out that the linear programming model based on clearing functions outperforms the iterative simulation-based one with respect to variable production plans and with respect to profit.

Supply network-wide master planning approaches are not well studied for the semiconductor manufacturing setting. We are only aware of the paper by Ponsignon and Mönch (2012). However, a clear limitation of our previous work is the assumption of a fixed lead time. In this paper, we make a first attempt to mitigate this assumption by considering an iterative simulation scheme. Note that the decision to look at an iterative scheme was influenced by the fact that we can reuse the simulation infrastructure that is described by Mönch and Zimmermann (2004) and Ponsignon and Mönch (2010).

3 ITERATIVE SIMULATION APPROACH

3.1 Iterative Scheme

The iterative scheme works as follows.

1. We denote the current iteration by i. Initialize $i := 1$. The maximal number of iterations is set to $iter_{\max} = 30$. Initialize the lead time $LT_{pm}^{(1)}$ for lots of product p in facility m by using historical data or results from simulation runs where the given demand is used to determine a release schedule. We denote the lead time used in iteration i by $LT_{pm}^{(i)}$.

2. Determine capacity consumption matrices $C_{pm}^{(i)}$ based on $LT_{pm}^{(i)}$, and solve the master planning problem using RA-MPSC. The resulting release schedule is denoted by $\tilde{x}_{pmt}^{(i)}$.
3. Use $\tilde{x}_{pmt}^{(i)}$ to perform three independent simulation runs. Take the mean for the cycle time obtained by the runs to estimate the cycle time $CT_{pm}^{(i)}$
4. If $i < iter_{\max}$ then update $LT_{pm}^{(i+1)} := (1-\alpha)LT_{pm}^{(i)} + \alpha\, CT_{pm}^{(i)}$, where $0 \le \alpha \le 1$ is a prescribed smoothing parameter. Round up $LT_{pm}^{(i+1)}$ to the next integer. In addition, set $i := i+1$ and go to Step 2. Otherwise, stop.

Note that we do not use a convergence condition as a termination criterion of the iterative scheme since we intend to investigate the evolution of the lead times in the long run. However, we limit the scheme to thirty iterations to keep the computational burden reasonable. A similar assumption is made in Irdem et al. (2010). The selection of the smoothing parameter α influences how much cycle time information from the simulation is taken into account when RA-MPSC is executed. Values for α close to one have the effect that almost the full cycle time information is used. Different values for α will be considered within our design of experiments.

3.2 Implementation Issues

We use the infrastructure for iterative simulation that is described by Mönch and Zimmermann (2004) and that was later extended to the simulation of supply chains by Ponsignon and Mönch (2010). The center point of this architecture is a blackboard-type data layer between an AutoSched AP simulation model of the one-stage supply chain and the master planning heuristic. Using notification functions of the simulation engine, the blackboard keeps track on completed lots to collect information related to the cycle times. The blackboard contains methods to calculate the capacity consumption matrices for each product and each facility. RA-MPSC and the blackboard are coded in the C++ programming language.

4 COMPUTATIONAL EXPERIMENTS

4.1 Design of Experiments

We are interested in examining the effect of three factors from the base and planning system on the performance of the iterative simulation scheme. The demand level (DL) is either low or high to influence the resource utilization. Three different settings for the initial lead times (ILT) of the products are considered. Accurate initial lead times result from Step 1 of the iterative scheme described in Subsection 3.1. Overestimated and under-estimated initial lead times are obtained by increasing and decreasing the accurate values by one period, respectively. Values for α are 0.20, 0.50, and 1.00. Similar settings for DL and α are considered in Irdem et al. (2010). A factorial design is used that leads to eighteen factor combinations. To limit the computing effort, one problem scenario is considered per factor combination. We perform three independent simulation replications for each combination. It allows mitigating the effect of variability in the base system on the results. Totally, 1620 simulation runs are carried out in the experiments. The design of experiments in use is summarized in Table 1.

The master plan typically has a horizon of six months divided into weekly buckets. We reduce the length of a single planning period to two days to mimic the situation that the cycle time in wafer fabs is often six weeks and weekly buckets are assumed. In addition, this approach decreases the computational effort.

Table 1: Design of Experiments

Factor	Level	Count
Base System		
Demand Level (DL)	low, high	2
Planning System		
Initial Lead Time (ILT)	accurate, over- and under-estimated	3
Smoothing parameter (α)	0.20, 0.50, 1.00	3
Total factor combinations		18
Number of problem scenarios per combination		1
Number of simulation replications per combination for a single iteration		3
Total number of simulation runs for a single iteration		54

The revenue and cost settings used by RA-MPSC are similar to the settings used in Ponsignon and Mönch (2012) to which a scaling down factor of 3.5 is applied due to the different time unit. The parameter settings of RA-MPSC are the same as in Ponsignon and Mönch (2012).

4.2 Simulation Model Used

The base system is represented by a simulation model. It consists of $m_{\max} = 4$ parallel wafer fabs. Each product can be processed in each of the four facilities. We consider $p_{\max} = 32$ products in all problem scenarios. The standard lot size is assumed to be 48 wafers in all facilities. We define the sequence of operations based on a simulation reference model that is derived from the MIMAC-I data set (MASMLab 1997). A process flow is assigned to each product that is a unique combination of sub-flows from the two products of the reference model. The processing of the products requires between 56 to 66 process steps depending on the fabrication routes. The process flow definition is identical in all facilities. Consequently, each product has the same raw process time in each wafer fab. We do not model setups and operators in the simulation model. The lithography work center is considered as the leading bottleneck in each facility due to the reentrant flows and the expensive machines. Hence, we set $b_{\max} = 1$. A similar assumption is made in Ponsignon and Mönch (2012). To keep the simulation model simple, the number of machines at the leading bottleneck is identical in all wafer fabs, i.e., the capacity of the base system is equally distributed across the facilities. The Earliest Due Date (EDD) dispatching rule is used to rank the lots in front of the bottleneck work centers. The First In First Out (FIFO) rule serves as a tie breaker. The single source of variability in the base system is the unplanned down time of the machines at the bottleneck work centers. The mean time to repair (MTTR) and mean time to failure (MTTF) distributions follow exponential distribution. We set MTTR=157 minutes and MTTF=2686 minutes. With this setting, the operation time of the machines is decreased by 5.85% on average.

A reduction approach is carried out to allow for decreasing the computational burden. We apply the method proposed in Hung and Leachman (1999) to downsize the degree of detail in the simulation model while achieving lot cycle time distributions that are comparable to those obtained with a detailed model. The reduced model focuses on a detailed modeling of the bottleneck resources. Non-critical machines are represented by stochastic delays using a Gamma distribution in the process flows of the lots. A similar approach is used in Ponsignon and Mönch (2010).

The model is initialized by performing three initial simulation runs with respect to the demand level under consideration, recording the number of lots in processing and in the queues, and adding the averaged WIP at the beginning of the first period of each simulation runs. The computational experiments are carried out on a computer equipped with a 2.5 GHz dual processor and 2.0 GB memory. The average computing time for performing thirty iterations of a single simulation run is around twenty-five minutes.

4.3 Results

We first investigate the convergence of the iterative scheme under different DL, ILT, and α factor levels. Therefore, we define the percentage mean absolute deviation (MAD) of the cycle time of product p in iteration i as $MAD_p^{(i)} := \frac{100\%}{m_{\max}} \cdot \sum_{m=1}^{m_{\max}} \left| CT_{pm}^{(i)} - \overline{CT}_{pm} \right| / \overline{CT}_{pm}$, where $CT_{pm}^{(i)}$ is the cycle time of product p averaged across all lots released from facility m during iteration i and $\overline{CT}_{pm} := \frac{1}{n} \sum_{i=1}^{iter_{\max}} CT_{pm}^{(i)}$. MAD values near zero suggest the convergence of the scheme. A similar measure is used in Hung and Leachman (1996) and Irdem et al. (2010). We follow the recommendation stated in the latter to consider the MAD values of the individual products. In the following, the MAD values are plotted as a function of the iterations.

Figure 2 shows the MAD values for the (DL=High, ILT=Accurate, α=0.20) case. The demand level setting leads to an average resource utilization of 92%. The overall maximum MAD value of 41.3% is obtained in the first iteration. One can see the continuous decrease of the MAD values in the first five iterations followed by a period of erratic fluctuations for some products. A rather stable level is observed after the thirteenth iteration. The maximum deviation from this iteration onwards reaches 10.8% while for the majority of the products their MAD values do not cross the 5% threshold.

Figure 3 plots the rounded product lead times used in RA-MPSC as a function of the iterations. For the purpose of this figure, the lead times are averaged across all facilities. The initial setting is four periods for all products. One sees the refinement of the lead times as a result of the iterative scheme, i.e., some product lead times converge to three periods while the others keep the four period setting.

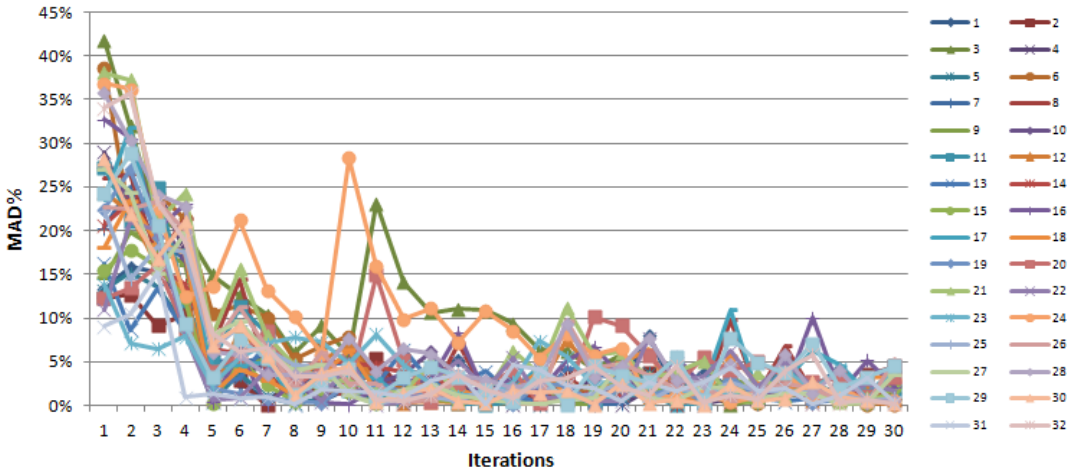

Figure 2: MAD in product cycle times for the (DL=High, ILT=Accurate, α=0.20) case.

We are interested in the effect of the ILT settings. The case of under-estimated ILT is shown in Figures 4 and 5. We observe higher MAD values in the first five iterations compared to the accurate case. The decrease of the MAD values follows a slower trend. All MAD values fall below the 10% threshold after 16 iterations and the average MAD value is slightly below 5%. The last lead time change occurs in the sixteenth occurrence. Hence, despite the initial bias of one period the iterative scheme seems to converge. A similar pattern can be observed for the cases with over-estimated ILT.

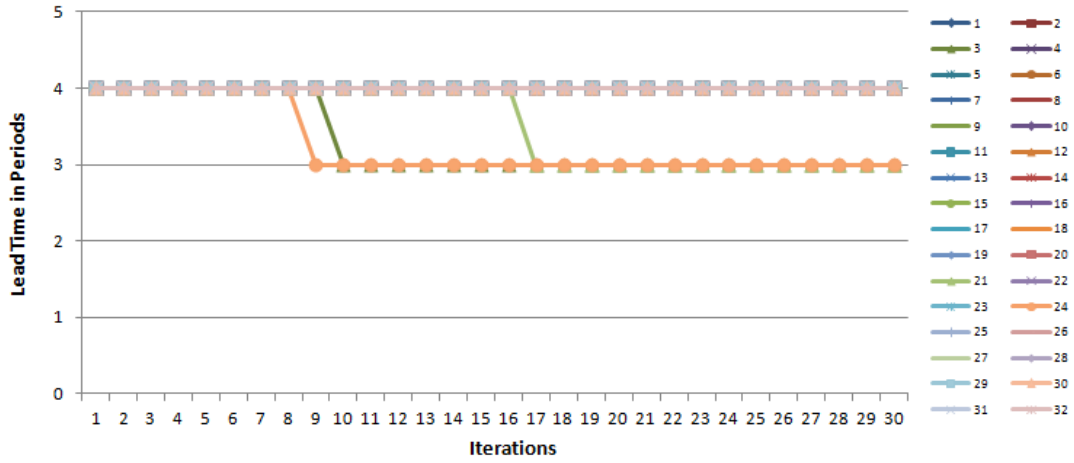

Figure 3: Product lead times for the (DL=High, ILT=Accurate, α=0.20) case.

The cases with a low demand level are characterized by lower MAD values at the beginning of the iterative scheme and a steep decrease in the first five iterations. The worst case is observed for the (DL=Low, ILT=Under-estimated, α=0.20) case where the maximum MAD value reaches 18% in the first iteration, and the last lead time change occurs at the twelfth iteration. The MAD values are below 4% from this iteration onwards. Hence, a convergence pattern is observed as well. This is not surprising since the average resource utilization of 54% leaves a certain flexibility to the base system to deal with different initial parameters.

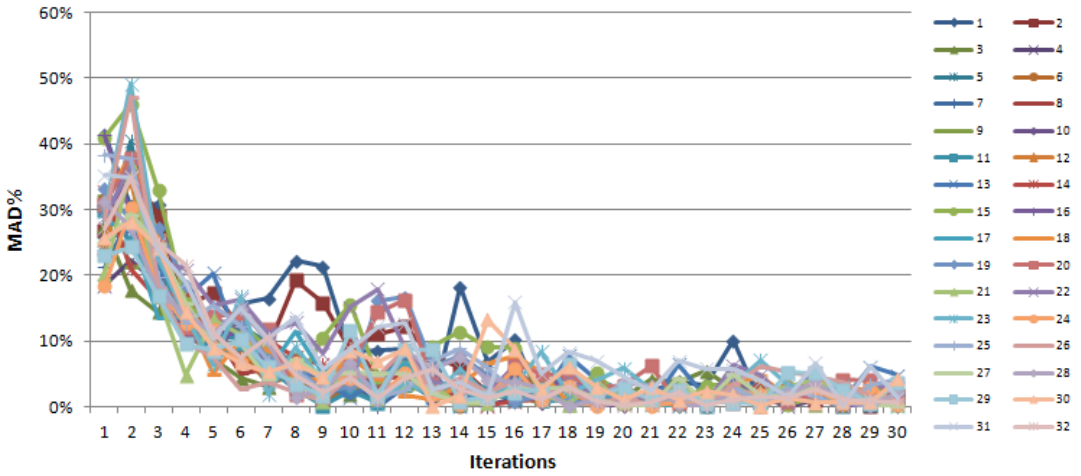

Figure 4: MAD in product cycle times for the (DL=High, ILT=Under-estimated, α=0.20) case.

We analyze the effect of different values for α. Figures 6 and 7 show the (DL=High, ILT=Accurate, α=0.50) case. A higher α value allows for taking more cycle time information from the simulation into account. We observe a much steeper decrease in the first three iterations than for the (DL=High, ILT=Accurate, α=0.20) case. Also the last lead time change occurs much earlier, i.e., in the seventh iteration. We conclude that the α=0.50 setting expedites the convergence of the iterative scheme.

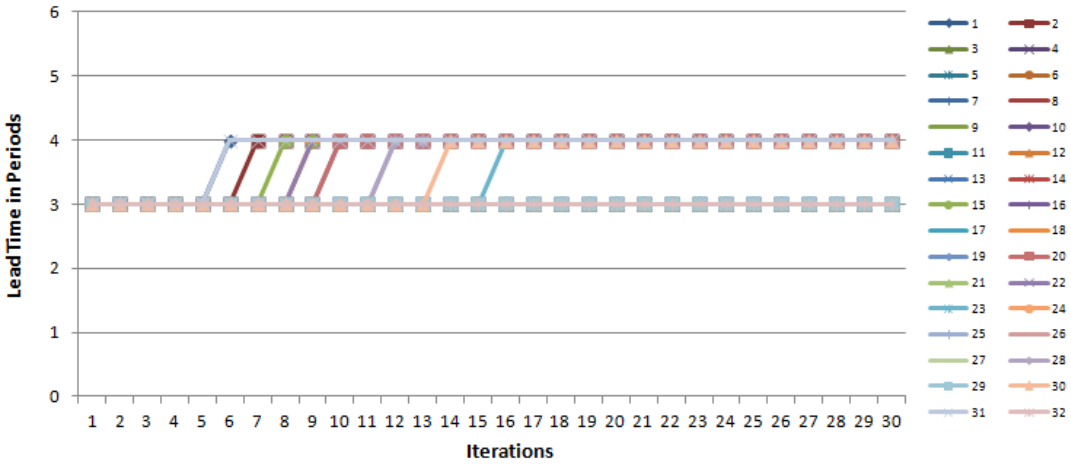

Figure 5: Product lead times for the (DL=High, ILT=Under-estimated, α=0.20) case.

On the other hand, the MAD values obtained for the cases with α=1.00 show high fluctuations and no convergence pattern. The worst case is obtained for the (DL=High, ILT=Under-estimated, α=1.00) case where the overall maximum MAD value reaches 48% in the twentieth iteration. Since more information is taken from the simulation, the convergence of the scheme is subject to the variability of the base system. Hence, it seems to exist a tradeoff between the convergent trend and the convergence speed.

Besides the convergence of the cycle times, it seems important to investigate the impact of the iterative scheme on the objective function values of RA-MPSC. In this situation, the MAD measure as $MAD^{(i)} := 100\% \cdot \left| F^{(i)} - \overline{F} \right| / \overline{F}$ where $F^{(i)}$ is the objective function value in iteration i and $\overline{F} := \frac{1}{n} \sum_{i=1}^{iter_{\max}} F^{(i)}$ is applied. Figure 8 plots the MAD values for the (DL=High, ILT=Accurate, α=0.20) case. One sees a similar pattern as in Figure 2, i.e., the MAD values decrease in the first six iterations, followed by erratic fluctuations between the tenth and the eighteenth iterations. After the twentieth iteration, the MAD value stays at a rather low level. A similar convergence behavior is observed for all other cases.

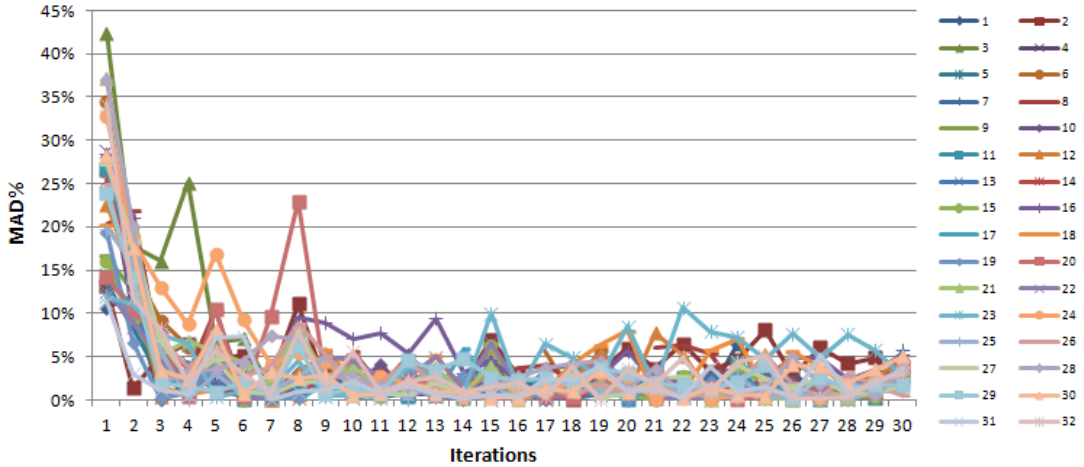

Figure 6: MAD in product cycle times for the (DL=High, ILT=Accurate, α=0.50) case.

To ensure the benefits of the iterative scheme, we investigate the throughput obtained from the simulation model as a function of the iterations. We apply the MAD measure described at the beginning of this subsection without taking absolute values of the summands. We get for each product and each iteration the difference between the realized throughput in all facilities and the average throughput across all iterations.

The mean deviations cumulated across the products are showed in Figure 9 for the (DL=High, ILT=Accurate, α=0.20) case. We observe higher positive deviations towards the last iteration than at the beginning of the iterative scheme, i.e., a higher throughput is reached.

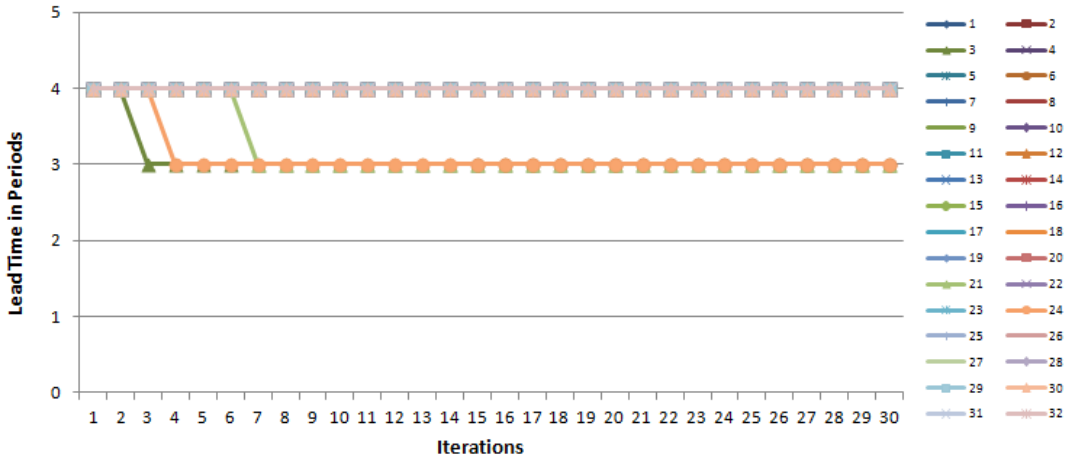

Figure 7: Product lead times for the (DL=High, ILT=Accurate, α=0.50) case.

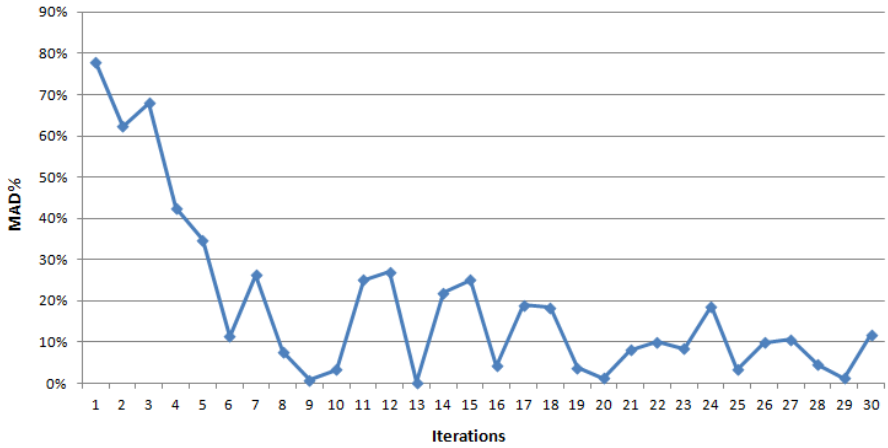

Figure 8: MAD in RA-MPSC objective function values for the (DL=High, ILT=Accurate, α=0.20) case.

Note that on average up to two percent throughput improvement is reached over all products. The trend clearly increases from the nineteenth iteration onwards. We can draw a parallel with Figure 8 that shows the lower MAD values starting from the same iteration. The higher throughput can be explained by the increasing number of products whose lead time is adjusted from four to three periods as shown in Figure 3. Lower lead times allow for more production requests being planned by RA-MPSC.

5 CONCLUSIONS AND FUTURE RESEARCH

In this paper, we discussed an iterative simulation scheme for master planning in a one-stage scaled-down semiconductor supply chain. The scheme alternates between a rather straightforward master planning heuristic and a reduced discrete-event simulation model of the supply chain. An AutoSched AP simulation is used that mimics important characteristics of wafer fabs. We demonstrated that the scheme converges after a small number of iterations and that it leads to less variable, more profitable production plans compared to planes obtained by the fixed lead time approach.

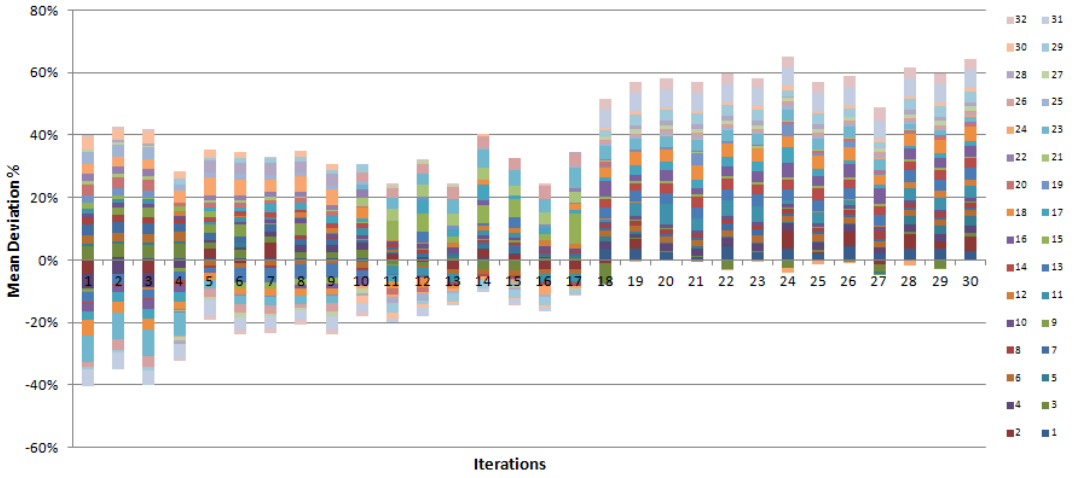

Figure 9: Mean deviation in realized throughput for the (DL=High, ILT=Accurate, α=0.20) case.

There are several directions for future research. First of all, we are interested in incorporating more sophisticated heuristics for master planning in our iterative scheme. In addition, more empirical testing of the approach is necessary. We are also plan to see whether we can use the coarse-grained simulation approach proposed by Ehm et al. (2011) to replace our current more detailed simulation models or not. Furthermore, it seems challenging to try to use clearing functions in a setting different from linear programming.

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