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INDUSTRIAL IMPLEMENTATION OF A DYNAMIC SAMPLING ALGORITHM IN SEMICONDUCTOR MANUFACTURING: APPROACH AND CHALLENGES

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ABSTRACT

In a worldwide environment, sustaining high yield with a minimum number of quality controls is key for manufacturing plants to remain competitive. In high-mix semiconductor plants, where more than 200 products are concurrently run, the complexity of designing efficient control plans comes from the larger amount of data and number of production parameters to handle. Several sampling algorithms were proposed in the literature, but most of them are seen impracticable when coming to an industrial implementation. In this paper, we present and discuss the industrial implementation of a dynamic sampling algorithm in a high-mix semiconductor plant. We describe how the sampling algorithm has been modified, and point out the set of questions that have been raised by the industrial program. Results indicate that more than 30% of control operations on lots could be avoided without increasing the material at risk in production.

1 INTRODUCTION

One of the strategies identified by semiconductor manufacturers to improve competiveness is to better manage controls throughout production (Mouli and Scott 2007). As controlling 100-percent is neither feasible nor interesting, dynamically identifying the right lots to control is critical to reduce costs without impacting product quality or increasing risks.

Several sampling algorithms are proposed in the literature (Purdy 2007; Sun and Johnson 2008). However, the specificity of each semiconductor manufacturer is such that most dynamic sampling algorithms proposed are too complex to industrialize. The IT infrastructure, the number of data to handle, the return on investment, or the company culture are some of factors that often lead to impracticability of many sampling algorithms.

In this paper, we present the industrial implementation of the dynamic sampling algorithm proposed by (Dauzère-Pérès et al. 2010) within the 300mm site of STMicroelectronics in Crolles, France. We first describe the sampling algorithm and financial metrics we developed to assess the potential gains. Then, we explain how the sampling algorithm has concretely been implemented using a mechanism introduced in (Nduhura Munga et al. 2011) for handling a large amount of data in short CPU times. At last, we discuss the various questions that have been raised by the industrialization program. We focus on defectivity

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controls and especially on the reduction of the material at risk, i.e. the potential loss in case a problem occurs. Financial metrics indicate a potential gain up to $1,000,000, and the industrial deployment showed that more than 30% of control operations on lots could be avoided without increasing the material at risk in production.

The paper is structured as follows. In section 2, we describe controls in semiconductor manufacturing, and clarify the position of our work. Section 3 presents the problem we address. Section 4 and Section 5 are devoted to the description of the dynamic sampling algorithm and its industrial implementation respectively. In section 6, we discuss the questions that have been raised when industrializing the approach. Section 7 concludes the paper and gives directions for further research.

2 CONTROLS IN SEMICONDUCTOR MANUFACTURING

In semiconductor manufacturing, controls are necessary evils because of the prohibitive amount of time required to manufacture a functional IC (Boussetta and Cross 2005). Different levels of controls exist depending on the point of view adopted (Bassetto and Siadat 2009). For each level of control, one or several types of controls can be defined. More generally, six main levels of controls can be defined (Wright 2001):

- Facilities or technical installations. The goal is to ensure the best possible environment for the fabrication of wafers: Clean room ambient characteristics (temperature, humidity, pressure, etc.), fluids, liquids, gases, energy (load, intensity, voltage), etc.
- Equipment sensors. To ensure efficient processing operations, all variations have to be detected and analyzed. For that, several types of sensors need to be placed on different production tools to trigger alarms and actions in manufacturing systems.
- **Fab or In-Line measurements**. This level of control groups measurements done on silicon wafers with a large variety of techniques: Ellipsometry, reflectivity, scanning electron microscopy, visual inspection, pixel to pixel comparison, resistivity, scatterometry, etc. The goal is to monitor both the process and the tool drifts.
- Parametric testing addresses basic parameters of electrical devices: Transistor voltage thresholds, leakage current, oxide breakdown voltage, etc.
- Final or functional tests aim at verifying that the semiconductor devices function properly.
- Physical characterization and wafer level reliability evaluate component life-time under various stressing conditions (humidity, temperature, corrosion, etc).

Among these six levels of controls, we focus on "**Fab or In-Line measurements**", and especially on defectivity controls that aim at detecting defects on wafers. Different types of defects exist (corrosion, particles, scratches, voids, extra-patterns, etc.) and they are mainly generated by production tools (Pepper et al. 2005). All production tools are concerned, since even the smallest tool has mechanical parts moving, and thus, a potential generation of defects on wafers. The complexity is therefore in the number of tools to control with a minimum number of control operations on lots. Additional factors such as the depth of control (one control operation may validate several tools) (Nduhura Munga et al. 2011) (Rodriguez-Verjan et al. 2011), the capture rate (all defects cannot be detected at any production stage) (Shantikumar 2007), the kill ratio (all defects do not have the same impacts on wafers), the product criticality (some products are more critical than others), the customer requirements, etc. contribute in increasing the complexity of designing efficient defectivity control plans.

3 PROBLEM DESCRIPTION

A control without real added value is waste of time and money. This is what has been highlighted within the framework of our works related to defectivity controls. Figure 1 shows an example that illustrates the drawbacks of static sampling for defectivity controls. Lots L2, L4, and L6 are flagged at the start of the production for defectivity controls after processing operations. The sampling plan is to control one lot every two lots, i.e. 50% of lots. However, the variability and factory dynamics are such that TOOL1 may

process all flagged lots i.e. L2, L4, L6 whereas TOOL2 does not process any. Consequences are an over-control for TOOL1 and lack-of-control for TOOL2.

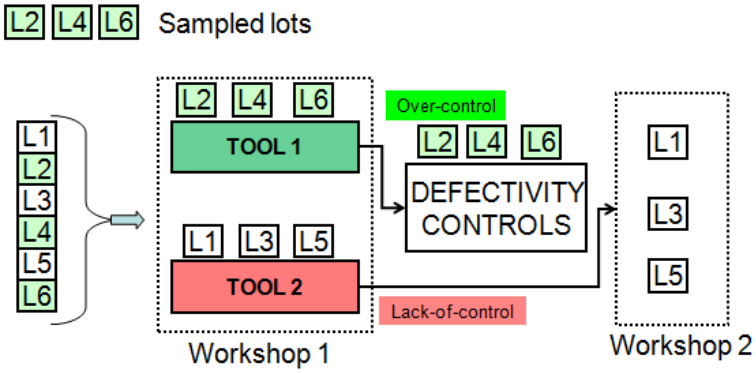

Figure 1: Drawbacks of Static Sampling

To solve this problem, lots should be dynamically selected in front of defectivity steps depending on the history of each lot. In the case illustrated in Figure 2, a dynamic sampling will lead to selecting, for example, lots L2, L3, and L6 to ensure a sampling rate of 50%.

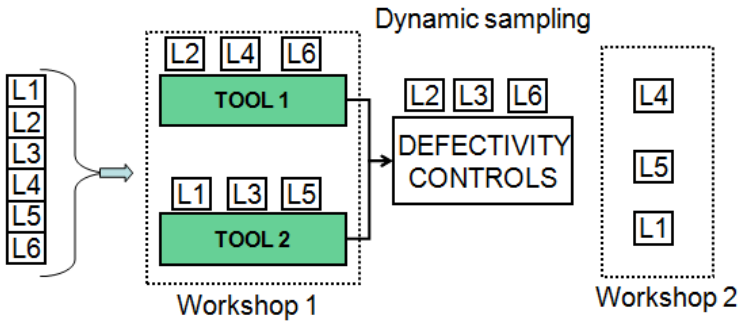

Figure 2: Dynamic Sampling

The challenge is in the dynamic selection of the best lots to control. A control operation on a lot (defectivity control) may cover several processing tools leading to a significant number of parameters to analyze. However, all tools and processing operations are not equivalent i.e. the criticality or priority vary depending on the tool, the processing operation, or the product type. Dynamically selecting the best lot to control implies the ability to compute and analyze in real-time all the information linked to both the lot history and production constraints. (Dauzère-Pérès et al. 2010) proposed an algorithm based on a formula that helps to give a weight to each lot arriving in front of inspection steps. The smaller the weight associated to a set of lots, the larger the priority of the lots in the set on inspection tools. This weight is called Global Sampling Indicator (GSI) and it is based on both the depth of control and tools criticality. The next section presents this GSI, its evaluation through simulations, and, financial metrics we developed to assess the potential gains before the industrial implementation.

4 DYNAMIC SAMPLING: GLOBAL SAMPLING INDICATOR (GSI)

This section first recalls the approach for dynamically sampling lots, and then explains the financial metrics that are used to evaluate the impact of a sampling strategy. For more information on the approach, see (Dauzère-Pérès et al. 2010).

4.1 GSI Sampling Algorithm

The dynamic sampling algorithm proposed by (Dauzère-Pérès et al. 2010) is based on a score or weight called GSI for Global Sampling Indicator. Each time a lot *l* is available for inspection and a set *S* of lots is already waiting to be inspected, a GSI score (and other parameters linked to the production constraints) is used to decide whether to include the lot *l* in the set *S* and skip another lot *l'* in S, or to skip the available lot *l*. The GSI score is linked to sets of lots. The aim is to define a weight that gives information on both the added value of an available lot *l* in term of risk reduction, and the added value of the available lot *l* within the set *S* of lots waiting to be inspected. For that, the sampling algorithm compares the GSI score of different sets obtained by removing *l'* and adding *l*, i.e. $S - \{l'\} \cup \{l\} \quad \forall l' \in S$, and the original set of lots without including the available lot *l*, i.e. *S*. The set with the minimum GSI score is selected, hence the decision of sampling or not the available lot *l*. The GSI score is given by:

$$GSI(S) = \sum_{r=1}^{R} \left[\left(\frac{NRV_r(S)}{IL_r} \right)^{(1/\beta)} + \left(\frac{NRV_r(S)}{IL_r} \right)^{\alpha} \right] \tag{1}$$

Where:

- R = Number of risk types.
- $NRV(S)$ = New risk value if lots in set S are inspected.
- IL_r = Inhibit Limit for risk type r, i.e. the maximum number of wafers that can be run between two inspections for risk r.
- α and β ($\alpha \geq 1$ and $\beta \geq 1$) are parameters that are used to put more (for α) or less(for β) emphasis on getting as far as possible from IL_r.

Before being industrialized, the GSI sampling algorithm had to be simulated, validated, and potential gains assessed. For that, a sampling simulator has been developed (Yugma et al. 2011) and Table 1 presents some of the statistics (provided by the simulator) that have been used to quantify the potential gains. Simulations on historical data were run over a period of three months, and the results are provided for the GSI sampling algorithm and actual fab sampling. In our experiments, the risk value is the W@R (Wafer at Risk), which is the number of wafers processed on production tools between two defectivity control operations, i.e. the material at risk. Reducing this number without increasing the number of controls has a direct impact on the insurance costs for the company, hence the gain in the product costs. Table 1 shows the number of sampled lots, measured lots and skipped lots, together with number of wafers above the Inhibit Limits, the average medium W@R and average maximum W@R for the production tools.

Table 1: Evaluating the GSI sampling algorithm.

	GSI sampling	**Fab Sampling**
Number of sampled lots	3.8*A	A
Number of measured lots	0.9*A	A
Number of skipped lots	2.9*A	0
Wafers above IL	**7,759,743**	**9,517,277**
Medium W@R (Average)	0.28*B	B
Maximum W@R (Average)	0.39*C	C

Note that, with a reduced number of measurements (0.9*A) compared to Fab sampling, the GSI sampling algorithm reduces the average medium W@R and average maximum W@R by 72% and 61% respectively. Among these six statistics, the number of wafers processed on production tools above the Inhibit Limits has been seen to be most practical for the assessment of financial gains as described in the next section.

4.2 Evaluating the GSI Sampling Algorithm: Financial Metrics

To evaluate the gains of the GSI sampling algorithm and therefore quantify the return on investment, we defined three different metrics. Among these three metrics, one has been seen to be more practical for our works related to defectivity controls. However, depending on the fab or the type of the risk addressed, one metric may be more suitable than another. The three metrics are:

1. The number of metrology tools that can be saved by using the GSI sampling algorithm. The idea is to compute the number of metrology tools required with the GSI sampling algorithm to obtain performance indicators that are as good as in current Fab sampling. However, as the goal is to not to reduce the number of measured lots but to reduce the number of measurements without added value, this first metric is not the most suitable.
2. The downtime costs incurred when Inhibit Limits are exceeded. The idea is to consider that a financial cost is incurred when a production tool is stopped because an Inhibit Limit is exceeded. The resulting downtime is a non productive time which costs money. We assume that the production tool stays down until the W@R becomes smaller than its corresponding Inhibit Limit. However, the problem of this second metric is that, in practice, a production tool will not always be stopped when its Inhibit Limit is exceeded. Therefore, this second metric is not the most relevant.
3. The risk related costs incurred when Inhibit Limits are exceeded. The idea is to consider that the risk of losing wafers increases when the W@R of a production tool is above its Inhibit Limit. Based on a probability of failure, it is possible to calculate how much money could be lost. **This last metric seems to be the most practical and was used to quantify the potential gains.**

Using results reported in Table 1, the potential gains were computed using the following formula:

$$Gain = (9{,}517{,}277 - 7{,}759{,}743) * P_{LOSS} * P_{\$}.$$

where P_{LOSS} represents the probability of losing wafers when a production tool is above its Inhibit Limit, and $P_{\$}$ is the average wafer cost. P_{LOSS} is linked to both the production environment and simulation period. Its value may thus be discussed depending on the processing operations and product types. In our works related to defectivity controls in the 300mm fab of STMicroelectronics, we considered a probability of *1/2000* and a wafer cost of *$1,500*, which gives:

$$Gain = (9{,}517{,}277 - 7{,}759{,}743) * (1/2000) * 1500 = \$1{,}318{,}150.$$

This significant potential gain, in addition to the performance indicators introduced in (Yugma et al. 2011), has been one the main motivations that led to the industrialization of the GSI sampling algorithm.

5 INDUSTRIAL IMPLEMENTATION

A survey of the literature (Nduhura Munga et al. 2012) showed that several sampling algorithms were impracticable for industrial implementation. This was also one of the main challenges for the GSI sampling algorithm. If simulations showed that significant gains could be achieved, additional types of evaluations had to be performed regarding the IT infrastructure, the data management and availability, the training of operators, the company culture, or the management of resources. The risk was to see potential savings completely eradicated by additional types of investments (IT, resources, trainings, etc.).

Another challenge that had to be faced was the type of risk to be mastered. Indeed, in the first evaluation of the GSI sampling algorithm, only the risk at the tool level (W@R, Wafer at Risk) was evaluated. However, in a high-mix environment as in the 300mm site of STMicroelectronics in Crolles, France, several types of risks related to defectivity controls need to be mastered: the number of wafers processed in the same chamber between two controls, the number of wafers at the same operation, with the same technology, recipe, resin, etc. The dynamic selection of lots should therefore ensure an optimal coverage of all of the types of risk. For that, the *IPC* (for the French “Indice Permanent par Contexte”, which means “Permanent Index per Context”) mechanism proposed in (Nduhura Munga et al. 2011) was industrialized to support the industrial implementation of the *GSI* sampling algorithm. The *IPC* is a counter linked to

several types of contexts (recipe, resin, technology, etc.). It has been introduced to simplify the risk computations. Each time a lot is processed on a production tool and verifies a given context, an *IPC* (IPC_l^c) is attached to the lot for the considered context as described in (Nduhura Munga et al. 2011). Using this IPC information, the *GSI* formula for a set *S* of lots was adapted as follows:

$$GSI(S) = \sum_{c=1}^{N} \left[\left(\frac{\underset{l \in S}{Min} \left(IPC_l^c - IPC_{LLM(c)}^c \right)}{IL_c} \right)^{(1/\beta)} + \left(\frac{\underset{l \in S}{Min} \left(IPC_l^c - IPC_{LLM(c)}^c \right)}{IL_c} \right)^{\alpha} \right] \quad (2)$$

where:

- N : Number of contexts,
- IPC_l^c : *IPC* of lot *l* for context *c*,
- $IPC_{LLM(c)}^c$: *IPC* of the lot Last Lot Measured (*LLM*) for context *c*, i.e. the last lot that has reduced the risk for context *c*,
- IL_c : Inhibit Limit for context *c*,
- α and β ($\alpha \geq 1$ and $\beta \geq 1$) are parameters that are used to put more (for α) or less(for β) emphasis on getting as far as possible from the Inhibit Limit.

Using the *IPC* information, the industrial implementation of the GSI sampling algorithm was considered as the only way to optimize the use of metrology tools by dynamically selecting the best lots to measure. Each context *c* (tool, chamber, recipe, resin, technology, etc.) is taken into account in the GSI formula, and the dynamic selection of lots aims at minimizing all the types of risks (contexts) in production.

The industrialization phase has been divided into three parts devoted to the sampling, skipping and scheduling of lots on metrology tools. The first part of the project focused on the skipping of lots in metrology and a first evaluation showed that more than 30% of control operations on lots could be released without increasing the risk in production. However, several questions have been raised by this transition from static to dynamic sampling. In the next section, we present some of these questions that constitute new directions for further research.

6 DISCUSSIONS AND PERSPECTIVES

The industrial implementation of the GSI sampling algorithm showed that a significant number of control operations on lots could be released without increasing the risk in production, hence a better management of metrology tools. However, modifying the sampling policy, i.e. replacing static sampling by dynamic sampling, changed the way engineers were working, leading to new problems that need to be solved. Here are some these new problems that are perspectives for further work:

1. **Defectivity tool qualifications**. Using start or static sampling, lots were flagged at the start of the production, i.e. the percentage of lots to be measured was defined at the start of production. Therefore, information on the products of the lots to be measured was known, and the qualifications of defectivity tools was taken into account to balance the measurement workload on the different types of defectivity tools. By dynamically selecting lots in front of metrology steps, there is no prior information on the set of lots to be measured. The consequence is that some defectivity tools may not be used enough if the right lots are not selected, and other defectivity tools may be too much loaded, leading to long cycle times for the lots waiting to be measured.
2. **Excursion management, i.e. when a process or tool falls out of specification**. Using static sampling, lots were flagged for regular measurements at some predefined steps. This means that, each time a problem was detected on a lot, it was easy to quickly identify the source of the problem by quantifying the added defects of each processing step. Using a dynamic sampling approach, the complexity of isolating the source of defects is increased, since lots are selected based

on the information they bring and not explicitly at all the metrology steps. An additional analysis must be performed before isolating the source of the excursion knowing that no production tool is stopped before this source is identified.

These problems show the types of complexity that need to be faced when trying to deploy a new strategy or approach within a high-mix semiconductor plant. As different types of organizations are called to work and collaborate (qualifications, sampling, scheduling, excursion management, production, etc.), each time a novel solution is proposed, the impact on the other activity types need to be clearly understood and assessed. Although this may vary from one company to another, significant efforts are required to convince and highlight the added value of the new solution. This is what has been experienced before industrially implementing the GSI sampling algorithm, explaining why many sampling algorithm proposed in the literature were impracticable.

7 CONCLUSION

In this paper, we presented and discussed the industrial implementation of a dynamic sampling algorithm within the 300mm site of STMicroelectronics in Crolles, France. We focused on defectivity controls and especially on the reduction of the material at risk, i.e. the potential loss in case a problems occurs. The dynamic sampling algorithm is based on a Global Sampling Indicator that evaluates the impact of measuring a set of lots and not only one lot. It has been industrialized using a Permanent Index per Context mechanism that help handling a very large amount of data in short CPU times. Results show a quick return on investment and a significant reduction of the number of control operations on lots without added value.

The industrial program has highlighted new problems that are interesting perspectives for further research. These new problems concern defectivity tool qualifications, the design of control plans and excursion management.

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REFERENCES

Bassetto, S., and A. Siadat. 2009. "Operational Methods for Improving Manufacturing Control Plans: Case Study in a Semiconductor Manufacturing." *Journal of Intelligent Manufacturing* 20: 55–65.

Boussetta, A., and A. J. Cross. 2005. "Adaptive Sampling Methodology for In-Line Defect Inspection." In *Proceedings of the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop,* Munich, Germany, 25–31.

Dauzère-Pérès, S., J.-L. Rouveyrol, C. Yugma, and P. Vialletelle. 2010. "A Smart Sampling Algorithm to Minimize Risk Dynamically." In *Proceedings of the 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference,* San Francisco, California, USA, 307–310.

Mouli, C., and M. J. Scott. 2007. "Adaptive Metrology Sampling Techniques Enabling Higher Precision in Variability Detection and Control." In *Proceedings of the 2007 IEEE/SEMI Advanced Semiconductor Manufacturing Conference,* Stresa, Italy, 12–17.

Nduhura Munga, J., S. Dauzère-Pérès, P. Vialletelle, and C. Yugma. 2011. "Dynamic Management of Controls in Semiconductor Manufacturing." In *Proceedings of the 2011 IEEE/SEMI Advanced Semiconductor Manufacturing Conference,* Saratoga Springs, New York, USA, 18–23.

Nduhura Munga, J., G. Rodriguez-Verjan, S. Dauzère-Pérès, C. Yugma, P. Vialletelle, and J. Pinaton. 2012. "A Literature Review on Sampling Techniques in Semiconductor Manufacturing." Working Paper, submitted.

Pepper, D., O. Moreau, and G. Hennion. 2005. "Inline Automated Defect Classification: a Novel Approach to Defect Management." In *Proceedings of the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop,* Munich, Germany, 43–48.

Purdy, M. 2007. "Dynamic, Weight-Based Sampling Algorithm." In *Proceedings of the 2007 IEEE International Symposium on Semiconductor Manufacturing,* Santa Clara, USA, 1–4.

Rodriguez-Verjan, G., S. Dauzère-Pérès, and J. Pinaton. 2011. "Impact of Control Plan Design on Tool Risk Management: A Simulation Study in Semiconductor Manufacturing." *MASM 2011* (7th *International Conference on Modeling and Analysis of Semiconductor Manufacturing),* In *Proceedings of the 2011 Winter Simulation Conference*, Edited by S. Jain, R. R. Creasey, J. Himmelspach, K. P. White, and M. Fu, 1918–1925. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

Shantikumar, J. G. 2007. "Effects of Capture Rate and Its Repeatability on Optimal Sampling Requirements in Semiconductor Manufacturing." In *Proceedings of the 2007 IEEE International Symposium on Semiconductor Manufacturing*, Santa Clara, USA, 1–6.

Sun, S., and K. Johnson. 2008. "Method and System for Determining Optimal Wafer Sampling in Real-Time Inline Monitoring and Experimental Design." In *Proceedings of the 2008 IEEE International Symposium on Semiconductor Manufacturing,* Tokyo, Japan, 44–47.

Wright, P. K. 2001. *21st Century Manufacturing.* 1st ed., Prenctice-Hall, Inc.

Yugma, C., S. Dauzère-Pérès, J.-L. Rouveyrol, and P. Vialletelle. 2011. "A Smart Sampling Scheduling and Skipping Simulator and its Evaluation on Real Data Sets." *MASM 2011* (7th *International Conference on Modeling and Analysis of Semiconductor Manufacturing),* In *Proceedings of the 2011 Winter Simulation Conference*, Edited by S. Jain, R. R. Creasey, J. Himmelspach, K. P. White, and M. Fu, 1908–1917. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

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