# Hybridization of NSGA-II with Greedy Re-assignment for Variation Tolerant Logic Mapping on Nano-scale Crossbar Architectures

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## ABSTRACT
There exit high variations among nano-devices in nano-electronic systems, owing to the extremely small size and the bottom-up self-assembly nanofabrication process. Therefore, it is important to develop logical function mapping techniques with the consideration of variation tolerance. In this paper, the variation tolerant logical mapping (VTLM) problem is treated as a multi-objective optimization problem (MOP), a hybridization of Non-dominated Sorting Genetic Algorithm II (NSGA-II) with a problem-specific local search is presented to solve the problem. The experiment results show that with the assistance of the problem-specific local search, the presented algorithm is effective, and can find better solutions than that without the local search.

## Categories and Subject Descriptors
I.2.8 [**Artificial Intelligence**]: Problem Solving, Control Methods, and Search.

## General Terms
Algorithms, Performance.

## Keywords
Nano-scale crossbar, NSGA-II, Local search, Hybridization, VTLM, Variation tolerant.

## 1. INTRODUCTION
Nano-scale crossbar architectures have been widely studied, for their great potential to be main building blocks in nano-electronic circuits. Nano-scale crossbar, an assembly of two or more parallel nano-scale wires array, has the merit of configurability and regularity.

As a result of the extremely small size of nano-devices and the bottom-up self-assembly nanofabrication process, it will be extremely hard to control the parameters of nano-devices precisely over design uniformity for future nano-electronic systems. The variation of the parameters will definitely cause the variation of the delay between input and output when lines are selected to work as input and output lines during the logical function mapping process. Such variation of delay will dramatically affect the performance of logical function module obtained from logical mapping. Thus, implement variation tolerant logical mapping on nano-scale crossbar architectures become a significant problem that must be studied. In this paper, a hybridization of NSGA-II with GR-inspired local search is proposed for VTLM.


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## 2. DEFINITION OF PROBLEM
The VTLM problem can be modeled as implementing a proper map between two matrices, VM and FM [2]. Matrix representing the delay information is called Variation Matrix. The logic function is represented by a binary Function Matrix. The mapping scheme can be expressed by an $n\times1$ Input Mapping Vector (IMV) and a $1\times m$ Output Mapping Vector (OMV) [2].

The delay of *ith* output $f_i$ is the sum of delays from relative inputs to the *ith* output. In [2], it is denoted by $C(f_i)$ and calculated as:

$$C(f_i)=\sum_{k=1}^{n} FM[k][i]\times VM[IMV[k]][OMV[i]] \quad (1)$$

The maximum path delay and output variation should be optimized simultaneously which are two major factors that affect variation tolerant of logic mapping. The two optimization objectives [1] are defined as follows:

$$objective\,1=\min(\max_i C(f_i)) \quad (2)$$

$$objective\,2=\min(\max_i C(f_i)-\min_i C(f_i)) \quad (3)$$

## 3. ALGORITHM
The proposed hybrid algorithm combines NSGA-II [6] with a problem-specific local search operator which is employed after a new population is created by using selection, crossover and mutation.

In the VTLM problem, IMV and OMV are encoded as two parallel chromosomes in one individual which are generated by random permutation in the initialization step.

The proposed approach chooses tournament selection, two-point crossover and adaptive mutation to generate new population.

**Local search**: Inspired by Greedy Re-assignment (GR) [3] which takes advantage of the greedy information extracted from the problem instances, a local search operator is designed for the VTLM problem. For this problem, output of function with more inputs should be mapped to the path with shorter average delay in the crossbar.

The pseudo code of the local search for VTLM is given in Algorithm 1. The greedy strength $k$ and individual learning intensity $n$ define the degree of exploration against exploitation in the algorithm. Greedy strength $k$ falls between 1 and $M$ (the length of chromosome), which should be chosen carefully. It means

doing nothing to the individual when $k$=1 and a certain rearrangement to the OMV of the individual when $k$=$M$. Individual learning intensity $n$ is an integer larger than zero.

**Algorithm 1:** GR-inspired Local Search

**Input:** Population at generation $t$, $Q_t'$; sorted number of VM's column, ***vo***; sorted number of FM's column, ***fo***; greedy strength [3], $k$; individual learning intensity, $t_l$; length of OMV, M;

**Output**: Population after local search at generation $t$, $Q_t$.

**Step 1**: Set individual learning count $n$=0.

**Step 2**: Select $k$ random number between 1 and $M$ to be a function output vector ***a***; find the vertical nanowire vector ***b***, $b[i] = OMV[a[i]]$.

**Step 3**: Sort vector ***a*** and ***b*** according vector ***fo*** and ***vo*** and create new vector ***a'*** and ***b'***.

**Step 4**: Do the re-assignment according to ***a'*** and ***b'***, $OMV[a'[i]] = b'[i]$.

**Step 5**: Set $n$=$n$+1. If $n$< $t_l$ go to Step 2.

**Step 6**: Stop.

## 4. EXPERIMENT AND RESULTS

Comparisons between NSGA-II and the HA (NSGA-II with GR-inspired LS) on two different sizes of mapping problem are shown to evaluate the effectiveness of the proposed method. In order to provide a quantitative comparison of results, two commonly used performance metrics, generational distance (GD) [4] and inverted generational distance (IGD) [5] are used and averaged over 30 trials.

In this experiment, the logic mapping problem of size 16×16 (D16) and 32×32 (D32) are considered. FM and VM are randomly generated as in [1]. Maximal number of function evaluations (FE) is the stopping criterion of the algorithms.

The population size is set to be 50 (100) for NSGA-II and the HA on D16 (D32). FE is set to be 2500 (100000) for both algorithms on D16 (D32), according to the evolutionary curves of pre-test. Greedy strength $k$ is set to be (1+$M$/8) empirically. We set optimal parameters $P_{cross}$ = 0.9, $P_{mut}$ = 0.2 and $P_{ls}$ = 0.9 experimentally by cross validation.

A set of experiments are conducted to analyze and compare the two methods. Fig. 1 and Fig. 2 show the transitions of GD and IGD for one instance of two mapping sizes. The others are omitted since all of them show similar behaviors regarding the same size.

In the two figures, we can see that the mean GD and IGD value obtained from HA are both lower than NSGA-II for the benchmark instances, which indicates that the non-dominated solutions of HA are closer to the true Pareto optimal front and have a better distribution. The GD (IGD) values using the HA algorithm for D16 and D32 are 48.72 (55.56) and 64.9 (61.9) percentage lower, respectively, than that of NSGA-II. This clearly indicates NSGA-II with GR-inspired local search has performed better than NSGA-II. It also indicates that problem-specific local search plays a great role on improving the performance of evolutionary algorithm for complex problems.

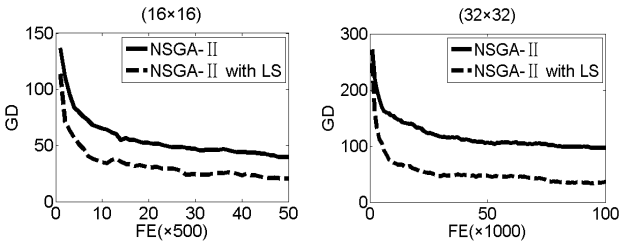


**Fig.1. Transitions of GD on benchmark instance**

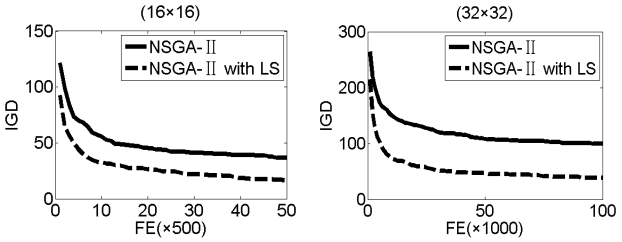


**Fig.2. Transitions of IGD on benchmark instance**

## 5. CONCLUSION

In this paper, a hybridization of NSGA-II and a problem-specific local search is presented for VTLM of nano-scale crossbar architectures. The effectiveness of the proposed method is shown by comparing results of NSGA-II and the hybrid algorithm on benchmark instances. Further research directions include a self-adaptive probability of local search and a diversity enhancement strategy for the hybrid algorithm.

## 6. ACKNOWLEDGMENTS

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