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Two Step Evolution Strategy for Device Motif BSIM Model Parameter Extraction

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***Abstract*— The modeling and simulation of semiconductor devices is a difficult and computationally intensive task. However the expense of fabrication and testing means that accurate modeling and simulation are crucial to the continued progress of the industry. To create these models and then perform the simulations requires parameters from accurate physical models to be obtained and then more abstract models created that can perform more complex circuit simulations. Device models (motifs) are created as a mitigation technique for improvement the circuit performance and as technology advances to help with the effects of transistor variability. In order to explore the characteristics of new device motifs on circuit designs, obtaining accurate and reliable device models becomes the first problem for designers. In this paper a Two Step Evolution Strategy (2SES) is proposed for device parameter model extraction. The proposed 2SES approach automatically extracts a set of parameters with respect to a specified device model. Compared with conventional mathematical extraction approach, 2SES is an efficient and accurate method to solve the parameter extraction problem and simultaneously addresses the fact of the mathematical extraction having the complexity of Multi-objective optimization. Compared with single step ES extract result, it is shown that the two-step ES extraction process continues improving generations by adjusting the optimisation parameters. Finally, an application of a new device motif on circuit design is given at end of the paper and compared against a standard device.**

I. INTRODUCTION

VLSI designers have to face new challenges caused by device scaling to deep sub-micron feature size causing for example stochastic variations. It is therefore becoming increasingly important to find design methodologies that more efficiently mitigate the impact of device parameter fluctuations. Some potential solutions are provided by materials and devices research [1]. Alternatively, novel device motifs using irregular layout style is an interesting avenue of research (such as O shape device motif depicted in Fig. 1). Layout style impacts the device performance and variability of transistors with nanometer scale features have been addressed in [1]–[4]. To explore the problem of device performance and its variability at the transistor level, accurate device-simulation analysis is essential and is regarded an efficient choice as directly fabricating chips is expensive and time-consuming in microelectronics industry.

Typically two simulations are provided to create the characteristic of device motifs needed for analysis, Technology Computer Aided Design (TCAD) simulation and SPICE simulation. TCAD simulates the electron-hole transportation in the device at the fundamental physical level using physical models. The advantage of TCAD simulation is that it avoids effects of factitious factors because of the characteristics of basic physical models, further improving accuracy of results [5]. Simultaneously, a fully 3D process and device simulation is easy to emulate and perform using TCAD tools. However, computational time has been sacrificed for the sake of obtaining accuracy, especially circuit level simulation. On the other hand, SPICE simulation also provides accurate device simulation by using many approximation equations (so called device compact model) rather than through fundamental physical models. The advantage of the compact model approach is that the computational time is much shorter than TCAD method, and particularly convenient for performing circuit simulation more than simple transistor simulation. However, the compact models, are constructed using many parameters, determining these parameters for new device motifs is a non-trivial process. To utilize the advantages of the two simulations, to achieve a precise device model and reflect the device behavior and prediction of the circuit outcome through accurate device motifs simulation, moving from TCAD to SPICE is critical. The 3D device motifs simulation is first performed to obtain I-V characteristics for Synopsys Sentaurus TCAD tool. Secondly, the compact models are extracted from TCAD simulated results. Once compact models have been obtained, circuits built by these device motifs compact model can be verified to ensure that circuits will function as intended [6]–[7].

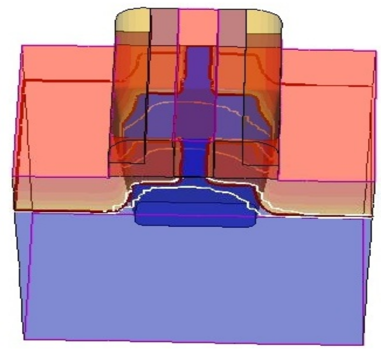
Fig. 1. 3D O shape device motif structure

Thus, obtaining a precise device motif's compact model is key in a new device simulation and evaluation. Since the

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MOSFET device scales to deep-submicron region, the Level 1 and Level 3 transistor models are no longer adequate to accurately model deep-submicron transistor behaviour [8]. A complex but accurate model from UC Berkeley, BSIM4, was developed to model sub-0.13 micron transistor behaviour that includes over 300 parameters and a set of equations. BSIM4 models provide precise device behaviour, though the difficulties of model parameter extraction increases as the number of parameters increase.

Conventional mathematical model extraction algorithm such as Levenberg-Marquardt (LM), have the limitation of a poor convergence without good initial conditions that heavily depends on the designers expertise and also the difficulty of simultaneous Multi-objective optimization [9]–[10]. The device model usually refers to several hundred I-V curve points. The extraction is a time consuming task to achieve a set of accurate parameter values with reasonable physical meaning. The ability of evolutionary algorithms to handle complex problems using Multi-objective optimization makes them an interesting candidate to solve this complex parameter extraction problem [9]–[13].

In this paper, we propose a Two Step Evolution Strategy (2SES) with a chromosome resizing mechanism to overcome the conventional method's drawbacks while balancing the use of computer resources. The rest of this paper is organized as follows: Section II describes the extraction procedures and the relation between parameters and I-V curve regions. The proposed ES with chromosome resizing mechanism is introduced in Section III. The simulation results and relative analysis are presented in Section IV. Finally, Section V provides some conclusions and suggests future work.

II. BSIM4 DC Parameter Analysis

This section provides a brief theoretical background of the BSIM4 DC model (MOSFET is shown in Fig. 2), which will serve as the foundation for understanding the relationship between the characteristics of MOSFET and BSIM model parameters. Understanding this link is critical for modelling device operations and characteristics via BSIM model.

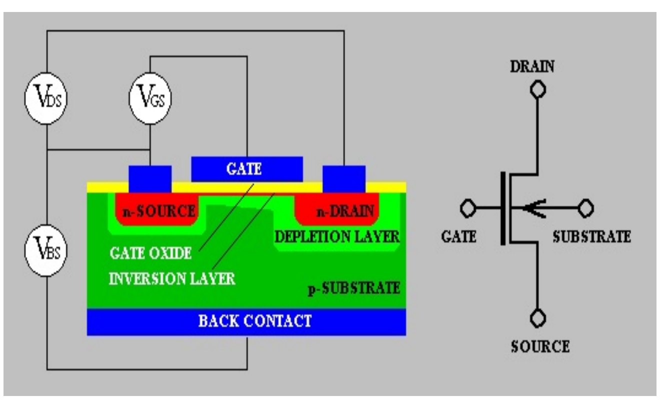


Fig. 2. Crosssection and circuit symbol of n-type MOSFET [14]

To obtain an explicit description of a device's electrical characteristics for DC analysis, it is necessary to analyze a

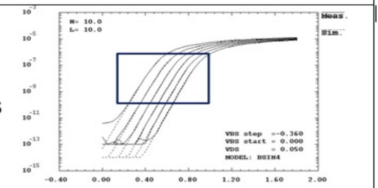
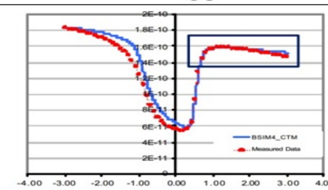
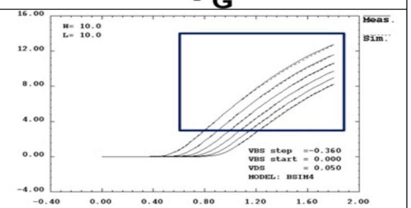
BSIM4 Parameter	Fitting Target
VTH0, K1, K2, DVTP0 ... (Threshold voltage) NFACTOR, VOFF, ... (Subthreshold Slop)	log I_{DS}  V_{GS}
TOXP, NGATE, (Quantum-mechanical charge layer thickness and poly gate depletion effect)	C_{GG}  V_G
U0, UA, UB, UC,(Mobility)	I_{DS}  V_{GS}

Fig. 3. A sensitivity relationship between the BSIM4 parameters and I-V curve fitting target

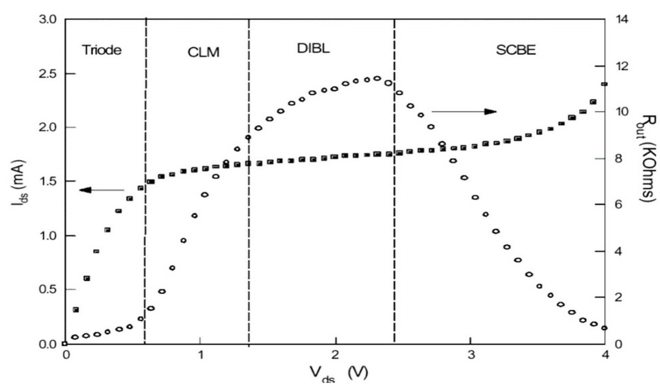


Fig. 4. Output Resistance vs. Drain-Source Voltage [8]

few key parameters such as threshold voltage, subthreshold region parameter, and channel mobility parameter. A sensitivity relationship between the BSIM4 parameters and I-V curve fitting is listed in Fig. 3. It is important to know the sensitivity of parameters on the curve fitting target to assist the extraction process and reduce optimization time. For example, the threshold voltage value, which is the most important electrical parameter in modeling MOSFETs, represents the onset of significant drain current flow. Besides threshold voltage, the subthreshold behavior is also very critical to the accuracy of device modeling. The drain current in subthreshold region is modeled by different parameters such as NFACTOR, CIT, etc [15].

TABLE I

BSIM MODEL PARAMETERS RELEVANT FOR THRESHOLD VOLTAGE, SUBTHRESHOLD SWING, AND MOBILITY [8]

Model Variable	Description
VTH0	long channel threshold voltage at Vbs = 0
K1	first-order body effect coefficient
K2	second-order body effect coefficient
K3	narrow width coefficient
DSUB	DIBL coefficient exponent in subthreshold region
ETA0	DIBL coefficient in the subthreshold region
ETAB	body-bias for the subthreshold DIBL effect
A0	Coefficient of channel length dependence of bulk charge effect
A1	First non-saturation effect parameter
A2	Second non-saturation factor
KETA	Body-bias coefficient of bulk charge effect
DVT0	first coefficient of short-channel effect on VTH
DVT0W	first coefficient of narrow-width effect on VTH for small channel length
DVT1	second coefficient of short-channel effect on VTH
DVT1W	Second coefficient of narrow width effect on Vth for small channel length
DVT2	body-bias coefficient of short-channel effect on VTH
DVT2W	body-bias coefficient of narrow-width effect on VTH for small channel length
NFACTOR	subthreshold swing factor
VOFF	Offset voltage in subthreshold region for large W and L
CIT	Interface trap capacitance
CDSC	Drain-Source to channel coupling capacitance
U0	Low-field mobility
UA	First-order mobility degradation coefficient due to vertical field
UB	Second-order mobility degradation coefficient

TABLE II

SATURATION REGION OUTPUT CONDUCTANCE PARAMETERS [8]

Model Variable	Description
DROUT	Channel-length dependence coefficient of the DIBL effect on output resistance
PSCBE1	First substrate current induced body-effect parameter
PSCBE2	Second substrate current induced body-effect coefficient
FPROUT	Effect of pocket implant on Rout degradation
PDITS	Impact of drain-induced Vth shift on Rout
PDITSD	Vds dependence of drain-induced Vth shift on Rout
PCLM	hannel length modulation parameter
PDIBLC1	First output resistance DIBL effect parameter
PDIBLC2	Second output resistance DIBL effect parameter
PDIBLCB	Body bias coefficient of output resistance DIBL effect
RDSW	Zero bias LDD resistance per unit width
PRWG	Gate-bias dependence of LDD resistance

In the drain current model, modelling mobility, is also significant to the accuracy of a MOSFET model. Table I lists the relevant parameters in the BSIM4 models and a brief description of each for threshold voltage, subthreshold swing and mobility.

Additionally, in order to achieve a better fit of the measured devices I-V curve and the curve generated by the extracted model, the I-V curve is broken into the triode and saturation regions which are depicted in Fig. 4. The first region is called triode or linear region at low drain voltage, where carrier velocity is not yet saturated [8]. An increasing drain voltage leads to a region that is dominated by carrier velocity saturation, thus it is called the saturation region. The saturation region is further divided into four sub-regions [8]. In the saturation region, device behaviour is governed by three different physical mechanisms and each of those mechanisms dominates the I-V curve in a specific place. Those mechanisms are Channel Length Modulation (CLM), Drain-Induced Barrier Lowering (DIBL), and Substrate-Current Induced Body Effect (SCBE). The subset of BSIM parameter (36) along with the relevant saturation regions that are used in the optimisation processes outlined in this paper are listed in Table II.

III. TWO STEP EVOLUTION STRATEGY

In an attempt to improve the accuracy and efficiency of the model extraction method a Two Step Evolution Strategy with chromosome resizing (2SES) is proposed in this paper. The properties of an ES are beneficial for achieving Multi-objective optimization important in this work [16]-[19]. To solve the problem of the traditional method achieving poor convergence without a good initial condition, a Two Step strategy is proposed to assist in obtaining good initial conditions, and then further optimizing them. Additionally, when good initial conditions are obtained, it also provides an optimization guide for later optimization. As the previous section discussed, a device's I-V curve is divided into several regions. Fitting curve target can be trimmed by adjusting chromosome parameter size. The flow chart of 2SES is depicted in Fig. 5.

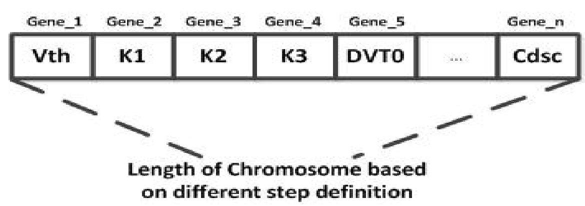


Fig. 6. The outline of the chromosome structure

A. Chromosome coding

The proposed algorithm employs an array consisting of floating-point numbers to encode chromosomes. Each floating-point number corresponds to a BSIM4 model parameter. Fig. 6 illustrates the outline of the chromosome structure. The design of the chromosome encoding strategy strongly depends on the properties of the MOSFET. This means that a chromosome needs at least 100 floating-point numbers to characterize the BSIM4 model. If all the parameters are encoded in the chromosome, there is no doubt that the huge search space puts a heavy burden on the algorithm, leading to a reduction of search efficiency. Consequently, only dominant core parameters are employed to build chromosomes in these experiment. In order to avoid

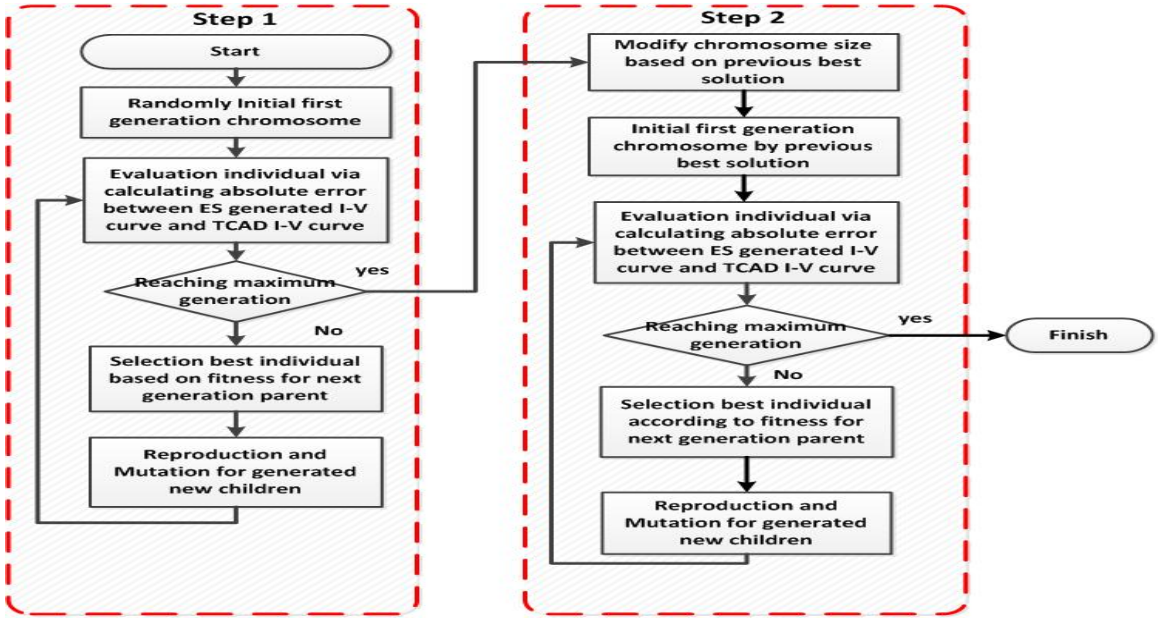


Fig. 5. The flow chart of 2SES

potential numerical problems, warnings or fatal errors being reported from simulation due to parameter falling outside the range limitations, the BSIM model parameters are restricted to specific ranges [11]. This means that each gene in the chromosome corresponding to BSIM parameter generated by 2SES is also restricted to a specific range. Since each parameter in the BSIM model has a different unit and range, all the parameters are chosen in the interval [0, 1], and are then mapped to their respective fields. This gene generation mechanism is calculated by the follow equation.

$$P_n = P_{nmin} + (P_{nmax} - P_{nmin}) \cdot \beta \tag{1}$$

Where β is a random floating-point number in the interval [0, 1], and P_{nmax} and P_{nmin} are the maximum and minimum value of n-th parameter respectively.

B. Genetic Operator

1) Mutation: Beginning with an initial parent generation in each iteration, a child is produced by randomly modifying the parent gene values. The mutation operation traditionally is performed by adding a normal distributed random value to the mutated gene [17]-[18]. The advantage of normal distribution is that has strongly local search ability [20]. However, the fitness value easily falls into local optimal. In order to enhance global search ability, the new gene is generated by adding the uniform distributed random value instead of the normal distributed random value. The mutation operation is described by follow equations:

$$\begin{cases} x_{k+1}(n) = x_k(n) + \xi_n, \\ \xi_n = random(P_{nmin}, P_{nmax}), \\ n = random(1, j), \end{cases} \tag{2}$$

Where $x_{k+1}(n)$ is the value of n-th parameter at k+1-th generation. ξ_n is a uniform distributed random value between the maximum and minimum vaule of n-th parameters. j is number of gene. For mutation operations, once a mutated genes value exceeds its range, then there is a need to regenerate a random number on the interval $[P_{nmin}, P_{nmax}]$.

Additionally, since the single gene mutation has better search ability and less computational overhead than the multi-genes mutation for the high-dimensional optimisation [20], the mutation operation is achieved by modifying a single gene value (shown in Fig. 7).

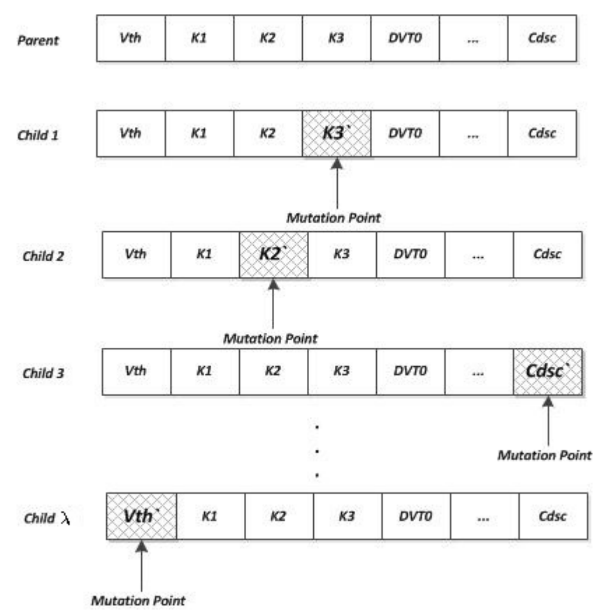


Fig. 7. Mutation operation of 2SES: The new gene is generated by adding the uniform distributed random value to the mutated gene value inherited from best solution on last generation, simultaneously this new generated gene value is limited within the specific value ranges. Once new gene falls into out of ranges, it will be re-generated.

2) Selection and Reproduction: After the mutation operation, all individuals are evaluated for breeding and the whole population is sorted according to fitness[17]-[18]. During the selection operation, a child always has a higher selection priority than the parents when both of them have same fitness value. To inherit elite solutions from the previous generation to the next generation, individuals with the best fitness values are directly copied into the next generation. A (1 + λ) strategy is used in these experiment. The algorithm can easily be extended to a (μ + λ) strategy, where μ is the number of parents and λ is the number of children.

3) Evaluation of Fitness: In this case, the difference between the TCAD measured curve and the ES generated curve is the essence of this problem. In general, root means square (RMS) is used for evaluation in such problems. However, RMS makes the fitting accuracy reduce drastically when the two evaluated values have different magnitude levels [11]. Drain current (I_d), especially, has no significant difference when gate voltage (V_g) is at low bias condition, but I_d is increased drastically as V_g becomes large [11]. Instead of RMS, the sum of absolute errors is used for evaluation. The sum of absolute errors between measured data and 2SES generated data is calculated using the following equation:

$$fitness = \sum_{m} \left| \frac{P_{ES}(m) - P_{measure}(m)}{P_{measure}(m)} \right| \quad (3)$$

Where m means the m-th measure point on the curve line. The actual drain current value at the m-th point is given by $P_{measure}(m)$. $P_{ES}(m)$ represents the simulated drain current value at the m-th point. In addition, model parameters extraction involves 10 I-V curve lines based on different V_d bias condition, each line has at 10 sampling point.

IV. Experiment and Simulation Results

In these experiment, the extraction is processed on an Intel i5 (4 cores), 8G RAM and Windows OS machine. Measured data of the device was obtained from TCAD 50nm NMOS device simulation results. Before extracting TCAD measured data of a device, a known SPICE model is extracted in a control experiment in order to verify that the methodology of 2SES algorithm is effective. Based on extraction result, the error between 2SES extracted model and SPICE reference model result is less than 1%. This validates that the 2SES can be seen as an effective method for device motifs extraction. In order to explore characteristic of the novel O shape device motif and regular device, models for each were extracted as illustrated in the follow section.

A. Regular Device Extraction

The 3D regular NMOS device structure (L = 50nm, and W = 80nm) is shown in Fig. 8. The evolutionary parameters are listed in Table III.

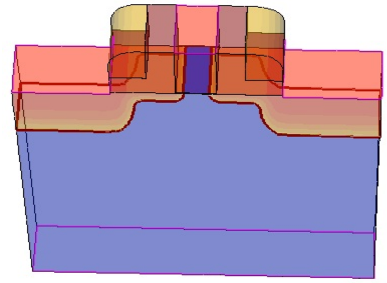


Fig. 8. 3D regular NMOS device structure

TABLE III
Two Step ES Parameters (regular device extraction)

ES parameters	value
Step number	1
Generation number	10,000
Population size	5 (1 + 4)
Mutation rate	1/24 (Mutation rate = 1/ n, n is number of chromosome)
Chromosome size	24 (Vth, k1, k2, k3, dvt0, dvt1, dvt2, dvt0w, dvt1w, dvt2w, u0, ua, ub, vsat, a0, a1, a2, keta, voff, eta0, etab, nfactor, cit, cdsc)
Step number	2
Generation number	10,000
Population size	5 (1 + 4)
Mutation rate	1/36 (Mutation rate = 1/ n, n is number of chromosome)
Chromosome size	36 (Vth, k1, k2, k3, dvt0, dvt1, dvt2, dvt0w, dvt1w, dvt2w, u0, ua, ub, vsat, a0, a1, a2, keta, voff, eta0, etab, nfactor, cit, cdsc, pdits, pditsd, pdiblc1, pdiblc2, drout, pclm, pdiblcb, fprout, delta, prwg, rdsw, dsub)

The extraction procedure is executed 10 times. The worst final generation fitness value at the second step of optimization is 14.14%. The best fitness value is 6.4%. Low fitness values are good in this case. Fig. 9 shows that the best solution of ES generated simulation curves in 10 runs (green dots) on the first step extraction. The sum of error of all curves between TCAD measured curves and ES generated simulation curves is 9.02%. As can be seen from the figure, the ES generated simulation curves fit well with TCAD measured curve at low drain region and has a weaker match in the saturation region. This result suggests the need to add relevant saturation region parameters on the second step optimization to achieve better fitting in the saturation region. In the second step optimization, the number of genes in a chromosome is raised to 36 from 24 genes. The second step optimization results are illustrated in Fig. 10. After the second step optimization, the sum of errors of all curves shown in Fig. 10 reduces to 6.4%.

To explain why we proposed Two Step strategy rather than a single step strategy: Both the single step and the first step of the Two Step strategy converge very quickly, any further improvement is then very slow. The Two Step strategy provides a potential way to further optimise the fitness more quickly via the chromosome resize mechanism which adjusts the optimization direction.

B. O Shape Device Motif Extraction

The measured data of the novel O shape device motif (L = 50nm and W = 160nm) also came from 3D TCAD simulation. The evolutionary parameters for the O shape device motif are listed in Table VI. To help with convergence,

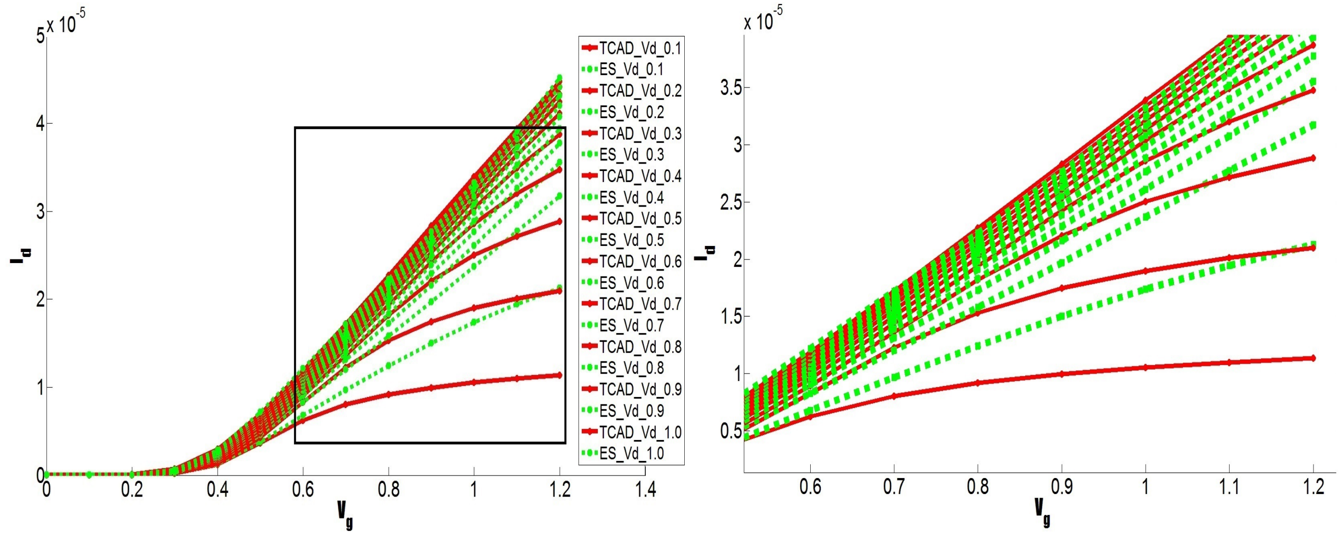


Fig. 9. The comparison between regular device TCAD measured curves (red) and ES generated simulation curves (green) for the best solution in 10 runs on the first step extraction. Two curves fit well in the triode region and have less match in the saturation region (shown in right sub-figure). It gives a suggestion to adjust optimization parameter size for the second step extraction.

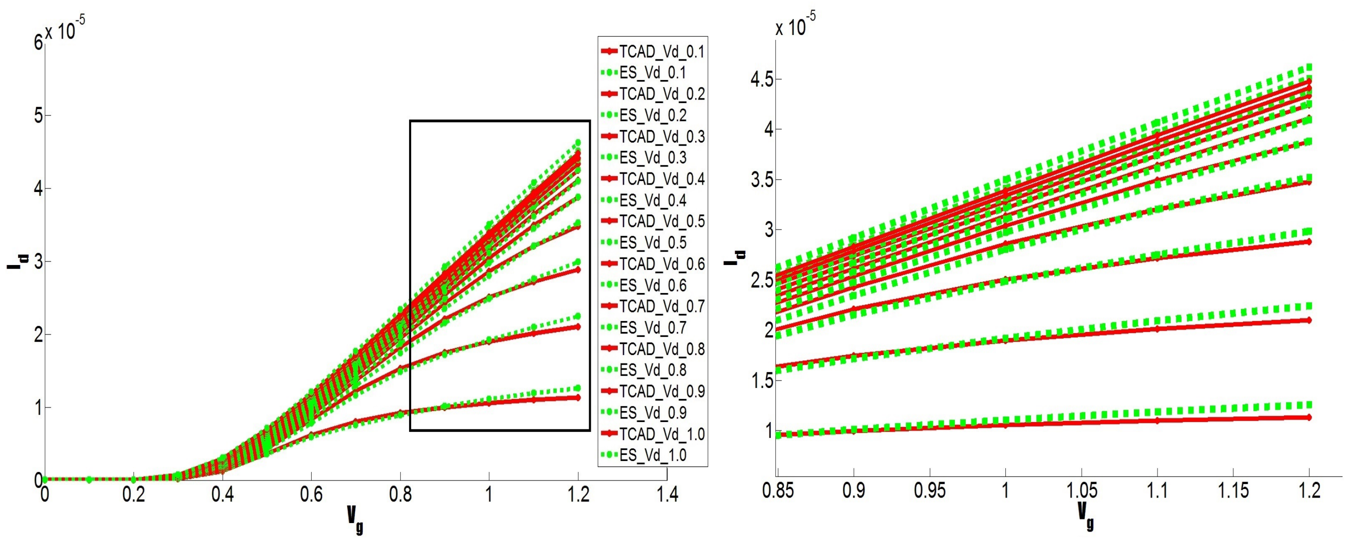


Fig. 10. The comparison between regular device TCAD measured curves (red) and ES generated simulation curves (green) for the best solution in 10 runs on the second step extraction. Two curves existing bigger error region is zoomed in the right sub-figure. After the second step extraction, two curves in the saturation region also have better match.

the generation number in this experiment was enlarged from 10,000 to 40,000, simultaneously; the population size is also extended to 20, (1 + 19), so as to assist the convergence process. The O shape device motif extraction also had 10 runs. The worst solution error is 11.19%. Here only the best solution of 10 runs is shown in Fig. 11 and shows the best device motif extracted result in 10 runs after first step extraction. The sum of error between TCAD measured data of O shape device motif and evolutionary generated data is 13.76%. This has similar properties to the regular device, in that it has better curve fitting in the triode region and mismatch in the saturation region, especially, curves with low drain bias. The second step extraction results show better accuracy between the TCAD simulated results and BSIM evolutionary extraction results (depicted in Fig. 12), where the fitness value finally converges to 6.22 %. Simultaneously, the O shape device motif extraction also has 10 runs by ES so as to compare with 2SES (summarized in Table V). The worst solution value extracted by ES is 63.48%, and the best solution is 40.02%.

To consider circuit operation for these new devices (rather than simply single devices) a comparison between the new O shaped device and a regular device was made for the construction of a NMOS inverter (schematic is shown in Fig. 13 and simulation result is illustrated in Fig. 14). As a result the benefit of device motif structure on circuit design, the

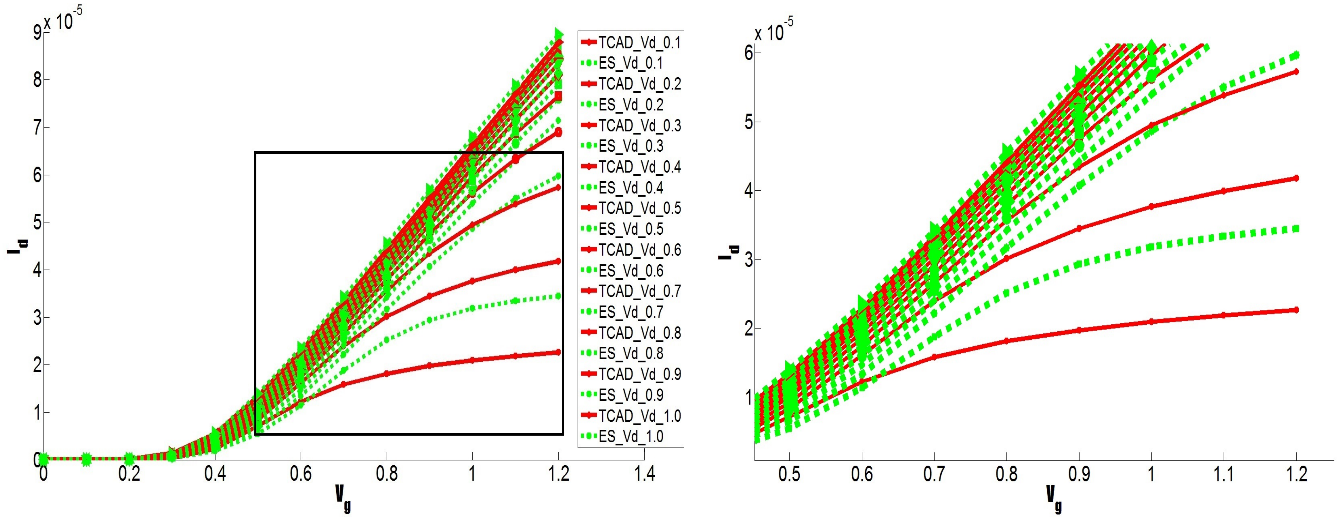


Fig. 11. The comparison between O shape device motif TCAD measured curves (red) and ES generated simulation curves (green) for the best solution in 10 runs on the first step extraction. O shape device motif extraction has similar properties to the regular device: it has better curve fitting in the triode region and mismatch in the saturation region (shown in right sub-figure).

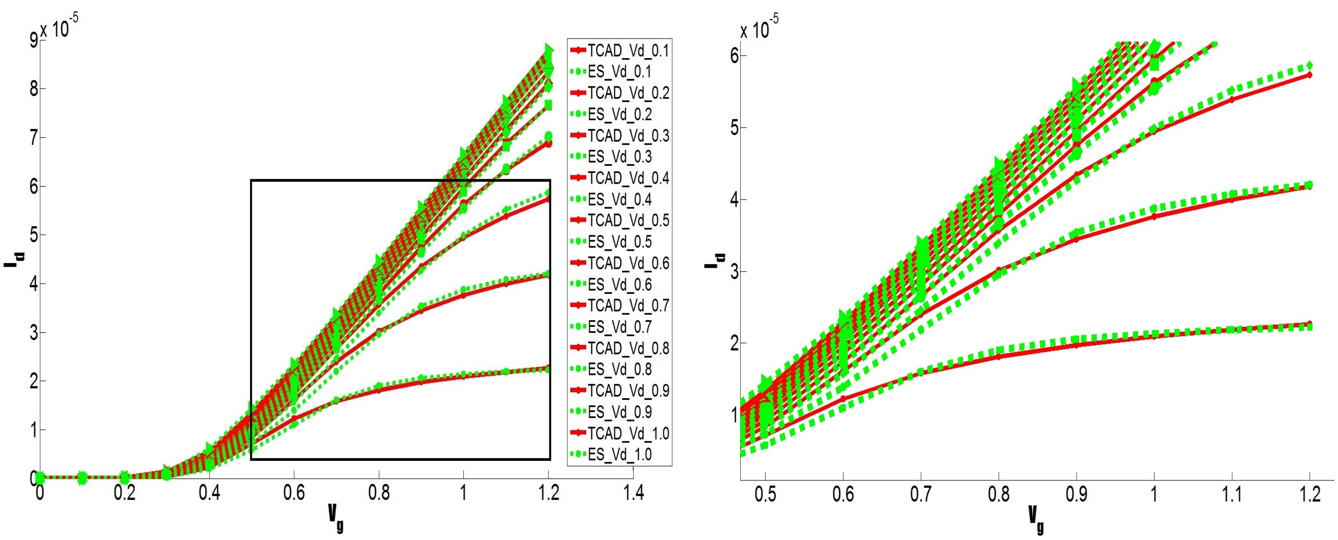


Fig. 12. The comparison between O shape device motif TCAD measured curves (red) and ES generated simulation curves (green) for the best solution in 10 runs on the second step extraction. Two curves existing bigger error region is zoomed in the right sub-figure. After the second step extraction, two curves fit well in the saturation region.

performance of the NMOS inverter circuit has been obviously improved using the novel O shape device motif.

V. Conclusions

This paper proposed employing a Two Step ES for MOSFET device motif BSIM4 model extraction. Although this work is only applied to single device extraction strategy, the method can easily be extended for a group device extraction with different geometries. The proposed 2SES approach automatically extracts device motif model parameters to obtain highly accurate results by tracking the shape variation of I-V curves. It takes less time to extract a feasible solutions then by conventional mathematical methods. In addition, the advantage of 2SES has kept the evolutionary improvement

TABLE IV
Two Step ES Parameters (O shape device extraction)

ES parameters	value
Step number	1
Generation number	40,000
Population size	20 (1 + 19)
Mutation rate	1/24
Chromosome size	24 (same as regular device)
Step number	2
Generation number	40,000
Population size	20 (1 + 19)
Mutation rate	1/36
Chromosome size	36 (same as regular device)

TABLE V
ES AND 2SES EXTRACTION COMPARISON

O shape device motif extraction	Best final fitness in 10 runs	Worst final fitness in 10 runs
Single Step ES	40.02%	63.48%
2SES	6.22%	11.19%

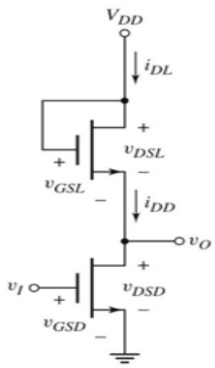


Fig. 13. The schematic of NMOS inverter

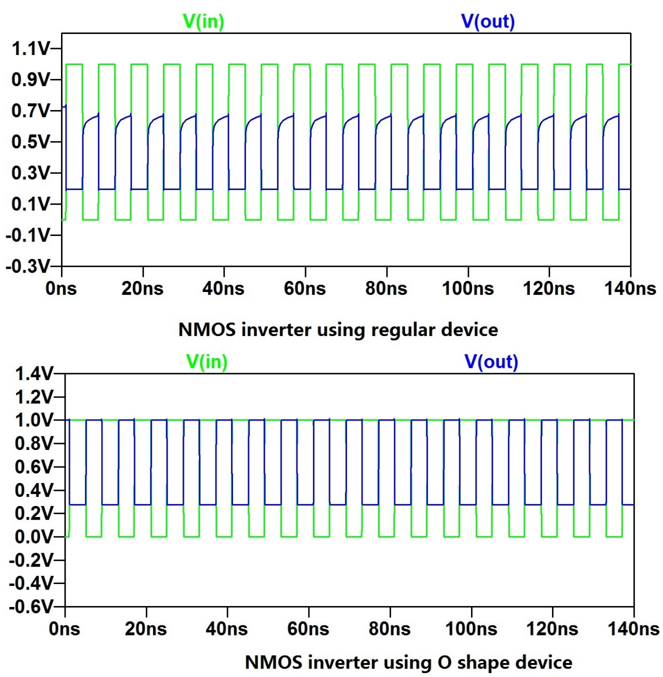


Fig. 14. The comparison NMOS inverter circuit simulation using O shape device motif (lower sub-figure) and using regular device(upper sub-figure)

by adjusting the optimization parameter. It may also promote convergence speed and limit cases where the algorithm is stuck in a local optima. The experiment results (summarized in Table V) show that 2SES is superior to single step strategy ES. Only NMOS device BSIM model is extracted and tested in this paper. In the future, in order to further explore the device motif technique, the PMOS device motif BSIM is planned and applied on circuit designs with NMOS device motif. Simultaneously, another planning branch is to extract TCAD device motif BSIM model with variability source (such as random discrete dopants and Line edge roughness), and mitigating the effect of transistor variability on circuit using the device motif technique.

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