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An Adjustable Memristor Model and Its Application in Small-world Neural Networks

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***Abstract*—This paper presents a novel mathematical model for the TiO_2 thin-film memristor device discovered by Hewlett-Packard (HP) labs. Our proposed model considers the boundary conditions and the nonlinear ionic drift effects by using a piecewise linear window function. Four adjustable parameters associated with the window function enable the model to capture complex dynamics of a physical HP memristor. Furthermore, we realize synaptic connections by utilizing the proposed memristor model and provide an implementation scheme for a small-world multilayer neural network. Simulation results are presented to validate the mathematical model and the performance of the neural network in nonlinear function approximation.**

Keywords—Memristor; PWL window function; Small-world model; function approximation

I. INTRODUCTION

The existence of memristor—the fourth fundamental circuit element, was predicted by Professor Chua in 1971 to complete the set of basic passive devices that already included resistor, inductor, and capacitor [1]. The missing constitutive relationship between flux-linkage and electric charge was thus found and formulized. Five years later a broader concept, memristive device, was introduced by Professors Chua and Kang to describe a wide range of devices with pinched hysteretic input and output dynamics [2]. However, it was only after the first physical implementation of memristor in a nanoscale double-layer TiO_2 thin-film by HP laboratory [3] that memristor and memristive devices started to attract increasing attentions from both academia and industry. Soon afterwards, various materials and devices demonstrating memristive characteristics were proposed, such as spintronic memristive systems [4].

Extensive research has been devoted to enable the computing and functional applications by using memristance (that is, memristor-resistance) as a new state variable. Novel attractive opportunities have been made in many systems, such as high-density nonvolatile resistive random access memory (RRAM) [5], ultra-high density Boolean logic and signal processing [6], reconfigurable nanoelectronic systems (e.g., FPGA) [7], nonvolatile VLSI computing [8], nonlinear circuit science (e.g., Chaos) [9], and neural inspired computing systems [10]. In this regard, an accurate mathematical model for memristors in nano-scale structure is important and necessary to support fast numerical analysis and computer-aided IC design [11].

The initial model of the HP memristor was provided by Strukov et al. [3]. It is a simple model considering only the linear form of ionic movement, which is normally called linear ionic drift model. Later on, this study was enriched by a number of more complex memristor models that take into account the nonlinear effects on ionic movement and the behaviors at device boundaries. Joglekar proposed to employ a single-valued window function in the model so as to capture the nonlinear effects and meet the boundary conditions [12]. However, such an approach brings in a serious "dead-lock" problem, that is, no external stimulus can drive a memristor any longer once it reaches one of the two boundaries. This scenario is also mentioned as boundary lock effect. In fact, all of the single-valued window functions will inevitably lead to this situation. In view of this, Biolek et al. presented a boundary-lock-effect-free model by using a switching window function [12]. The model includes the nonlinear effects at only one boundary each time. Moreover, the two-valued window function can cause different increments and decrements corresponding to the excitations with the same amplitude but at opposite polarities, i.e., charge-induced-shift effects. Recently, Corinto et al. created a one-valued switching window function and proposed a boundary condition-based model (BCM) based on it [13]. Unfortunately, no nonlinear effects can be reflected with this memristor model. In other words, it is indeed a boundary-effect-free linear model.

After studying the advantages and drawbacks of these existing approaches, we propose a more flexible *PWL model* by utilizing a piecewise linear window function. The PWL model can approximately captures all the behaviors of the HP memristor provided by several typical models. Besides the current passing through the memristor, four tunable parameters are introduced to characterize the window function. These parameters together make the PWL model transform smoothly between the linear and the nonlinear ionic drift cases.

As a highly simplified abstract of brain nervous systems, an artificial neural network is usually developed to execute some complex computing tasks. Such a network is constituted by a number of nodes representing neurons connected by links in

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certain structures, such as forward, feedback, fully-connected, single-layered, or multilayer. Nevertheless, these extensively studied neural network models own a common property — the complete connections among the neurons nearby. In fact, some randomness existing in brain neural networks has been discovered: the connections between a pair of neurons and the states of these neurons could change by following certain probabilities. Therefore, much enthusiasm has been shown on developing novel network model rather than the two existing limited network structures, i.e., the regular network and the random network.

Recent discoveries have demonstrated that the real biological nervous systems possess the sparse connectivity of complex networks as well as small-world effect and scale-free property [14-15] that have been observed in microscopic anatomical scale [16-18]. The so-called small-world model is generated by adding some randomness in a regular network. It has greater local interconnectivity than a random network but the average path length between any pair of nodes is smaller than that of a regular network. The combination of large clustering and short path length makes it an attractive model capable of specialized processing in local neighborhoods and distributed processing over the entire network. In this work, we present an implementation scheme for a small-world model based multiple neural network by utilizing the PWL memristor as synaptic connections. The findings of the study may promote the further development of the neural networks, especially in hardware realization.

This paper is organized as follows. We first present the PWL model and describe its unique features in Section II. The validation of the proposed model is conducted in Section III through numerical simulations and comparison with several typical models. In Section IV, a SPICE realization of the theoretical memristor model is provided, which can be directly applied to numerical analysis and computer-aided IC design. In Section V, we investigate the usage of the PWL model in a small-world neural network as a case study. Finally, Section VI concludes the whole paper.

II. THE PWL MEMRISTOR MODEL

The HP memristor is a nanoscale device in a structure of platinum contact−titanium dioxide film−platinum contact. In particular, the titanium dioxide film is divided into a TiO_2 layer with low conductivity and a TiO_{2-x} layer of high conductivity. The memristive effect is achieved by moving the doping front, that is, the interface between the TiO_2 and the TiO_{2-x} layer. Let D and W be the thickness of the titanium dioxide double-layer film and the TiO_{2-x} layer, respectively, R_H and R_L respectively denote the high resistance state and the low resistance state. The overall memristance can be expressed as

$$M(x) = x \cdot R_L + (1-x) \cdot R_H , \tag{1}$$

where $x \in [0, 1]$ represents the time-dependent relative doping front position, that is

$$x(t) = W(t) / D . \tag{2}$$

$$\frac{dx(t)}{dt} = \mu_v \cdot \frac{R_L}{D^2} \cdot i(t) \cdot f(x(t), i(t)) , \tag{3}$$

where μ_v is the equivalent ionic mobility in $m^2 s^{-1} V^{-1}$. A switching piecewise linear window function $f(\cdot)$ is designed to guarantee the boundary conditions, that is, $M \in [R_L \; R_H]$, and the nonlinearity in doping front movement near boundaries, as follows:

$$f(x, i) = stp(i - i_{th1}) \cdot f_1(x) + stp(-i - i_{th0}) \cdot f_2(x) , \tag{4}$$

where

$$stp(y) = \begin{cases} 1, & y > 0 \\ 0, & y \le 0 \end{cases}, \tag{5}$$

$$f_1(x) = \begin{cases} \dfrac{1-g_1}{c_1} \cdot x + g_1, & 0 \le x < c_1 \\ 1, & c_1 \le x \le c_2 \\ \dfrac{1}{c_2 - 1} \cdot x - \dfrac{1}{c_2 - 1}, & c_2 < x \le 1 \end{cases}, \tag{6}$$

and

$$f_2(x) = \begin{cases} \dfrac{1}{c_1} \cdot x, & 0 \le x < c_1 \\ 1, & c_1 \le x \le c_2 \\ \dfrac{g_2 - 1}{1 - c_2} \cdot x + \dfrac{1 - g_2 \cdot c_2}{1 - c_2}, & c_2 < x \le 1 \end{cases}. \tag{7}$$

where non-negative i_{th1} and i_{th0} denotes the current thresholds only over which the external excitation can change the memristor state. Parameters c_1 and c_2 are used to determine the regions of the nonlinear ionic drift and the linear ionic drift in the form of state variable x, i.e., $\{x \mid (0 \le x < c1) \cup \quad \le 1)\}$ and $\{x \mid c1 \le x \le c2\}$, respectively. g_1 and g_2 are the controlling parameters respectively reflecting the coincidence degree of the characteristics of $f_1(\cdot)$ and $f_2(\cdot)$.

Theoretically, the ranges of these four parameters shall satisfy

$$0 \le c_1 \le c_2 \le 1 , \text{ and} \tag{8}$$

$$g_1, g_2 \in [0, 1] . \tag{9}$$

In particular, if $c_1 = 0$ and $c_2 = g_1 = g_2 = 1$, then

$$f(x) \equiv 1 , \tag{10}$$

which leads to the linear ionic drift model, which is too simple to capture some practical properties. Instead, we restrict the four parameters in an open interval of $(0, 1)$ in this work.

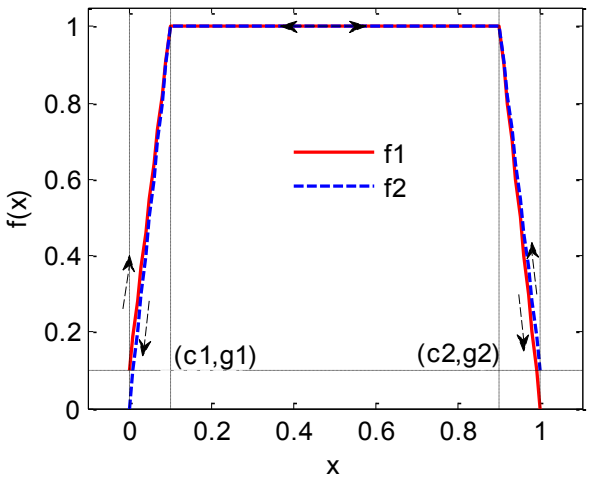

Fig. 1. The proposed PWL window function coined by (4)-(7).

Fig. 1 shows characteristics of the proposed PWL window function. To our best knowledge, the velocity of the doping front movement becomes smaller as the doping front moves near the two boundaries than that around the middle of the device. In other words, the ionic drift is depressed when approaching device edges. In the PWL model, we use the four parameters to model such nonlinear effects. Especially, parameters g_1 and g_2 denote the starting points of $f_1(\cdot)$ and $f_2(\cdot)$, respectively. To avoid the dead-lock problem at boundaries, g_1 and g_2 cannot be zero. However, such a constraint unavoidably causes the charge-induced-drifting effect due to the asymmetry of the switching window function. Fortunately, we can alleviate the effect to an acceptable level by setting g_1 and g_2 with small enough values. This is a big difference of our PWL model from Biolek's model. Other possible solutions include controlling the external excitation or taking some resetting operations.

Remarks: the window function cannot be continuous if the memristor model is expected to reflect the boundary conditions meanwhile escaping from the dead-lock problem.

III. Model Validation

We verify characteristics of the proposed PWL model by means of typical numerical analysis in this section. In all the following simulations, we set $R_L = 100\,\Omega$, $D = 10^{-8}nm$, and $\mu_v = 10^{-14}\,\mathrm{m^2 s^{-1} V^{-1}}$. In order to compare with other typical models in the same conditions, we set $v_{th1} = v_{th0} = 0$.

A. Normal Operating Mode

The normal operating mode for a memristor denotes the condition under which the internal state variable is always guaranteed within an effective range, that is, $x(t) \in (0, 1)$. Thus, the memristor exhibits the normal memristive effects.

Fig. 2 shows the frequency-dependent current-voltage (*I-V*) characteristics of a memristor subject to a periodic voltage excitation. Under the low-frequency excitation, an obvious pinched hysteresis loop is demonstrated. Under the condition with a higher frequency, however, the hysteresis loop collapses and the memristor degenerates into a normal resistor with a constant resistance state. Similar observation was obtained in Fig. 2(b) in [3].

In this simulation, the excitation voltage follow the form of $v(t) = \sin(2\pi f_0 t)$. In Fig. 2, the simulated *I-V* characteristics when $f_0 = 1Hz$ and $f_0 = 10Hz$ are represented by the dashed loop and the solid line, respectively. The parameters of the memristor are set as: $R_H = 16k\Omega$, $c_1 = 0.1$, $c_2 = 0.9$, and $g_1 = g_2 = 0.01$. Changing the excitation to $v(t) = \pm 1.5\sin^2(2\pi t)$ and increasing $R_H = 38k\Omega$ can result in the multiple-loop hysteresis curves similar to those in Fig. 2(c) in [3], as shown in Fig. 3.

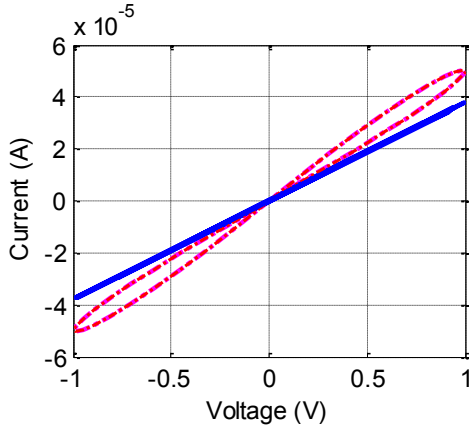

Fig. 2. Typical current-voltage pinched hysteresis loops under excitation $v(t) = \sin(2\pi f_0)$. The dashed loop is for $f_0 = 1Hz$ and the solid line is for $f_0 = 10Hz$.

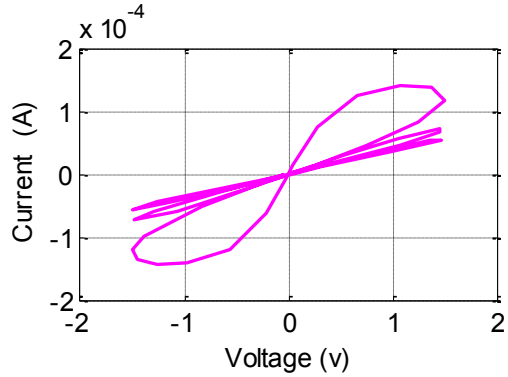

Fig. 3. Multiple-pinched-loop hysteresis curves under the applied voltage $v(t) = \pm 1.5\sin^2(2\pi t)$.

B. Special Operating Modes

The PWL model can successfully exhibit special properties when a memristor is working under certain abnormal working

conditions, such as small R_H/R_L ratio and big external excitations. Fig. 4 and Fig. 5 present the simulation results of special operating modes. The simulation with dynamic negative differential resistance (NDR) is given in Fig. 4(a), where $R_H = 12.5k\Omega$, $c_1 = 0.1$, $c_2 = 0.9$, and $g_1 = g_2 = 0.001$. For comparison purpose, Fig. 4(b) shows the result without NDR by changing the simulation setup to $R_H = 5k\Omega$, $c_1 = 0.1$, $c_2 = 0.9$, and $g_1 = g_2 = 0.001$. The simulations of Fig. 4(a) and (b) indicate that the NDR is not an intrinsic property of memristor but depending on the device parameters and external excitations. Fig. 5 demonstrates that the PWL model can successfully model the nonlinear ionic drift behaviors of a physical memristor. Here, the parameters of the memristor are set to be: $R_H = 5k\Omega$, $c_1 = 0.2$, $c_2 = 0.8$, and $g_1 = g_2 = 0.01$.

Under all the above cases, the hard-switching effect can be observe as the doping front approaches either of the two boundaries ($x(t) \to 0$ or $x(t) \to 1$). All these simulations are perfectly in line with the results in Fig. 3 (a)-(c) of [3], validating the accuracy of the proposed PWL model.

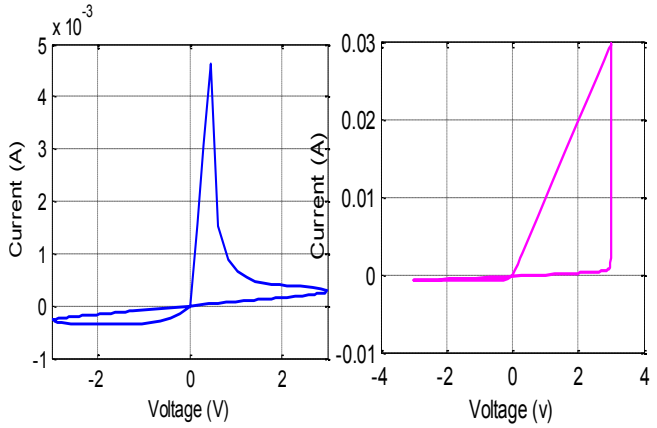

Fig. 4. Memristor current-voltage curves under $v(t) = -3\sin(2\pi t)$. (a) The simulation with dynamic negative differential resistance, and (b) the simulation without dynamic negative differential resistance.

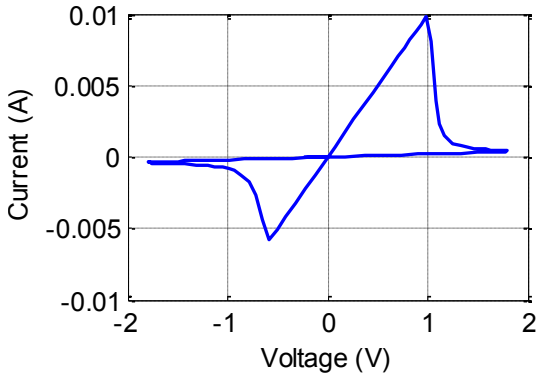

Fig. 5. Simulation governed by nonlinear ionic drift of the memristor under $v(t) = -1.8\sin(2\pi t)$.

TABLE I
COMPARISONS OF THE TYPICAL MEMRISTOR MODELS

Effects	Linear [3]	Joglekar [12]	Biolek [12]	Corinto [13]	PWL (this work)
Drifting Effect	No	No	Much	No	Less
Boundary Lock Effect	\	Yes	No	No	No
Boundary Conditions	No	Yes	Yes	Yes	Yes
Slow-down Effect	No	Yes	Yes	No	Yes

In TABLE I, we summarize and compare the properties of several typical memristor models. Here, the drifting effect represents the charge-induced drifting-effect, the boundary lock effect stands for the dead-lock problem, and slow-down effect denotes the slower doping front movement or the nonlinear ionic drift effect. The proposed PWL model possesses composite advantages over all these typical models. What's more, the PWL model can express all of the other models by properly adjusting its window function parameters.

IV. SPICE IMPLEMENTATION OF THE PWL MODEL

SPICE modeling is an effective method in analyzing device characteristics and observing electrical properties. In this work, a SPICE model is built up based on the theoretical equations given in Section II. TABLE II describes the SPICE sub-circuit. Applying an AC voltage source across the memristor device in SPICE simulation, we can obtain a footprint hysteresis loop on the current and voltage plane presented in Fig. 6, which is consistent with the simulation result of Fig. 5(b) in [12].

TABLE II
SUB-CIRCUIT DESCRIPTION OF THE PROPOSED MEMRISTOR MODEL

```
* The Memristor model with PWL window function
.SUBCKT HMemristor Plus Minus PARAMS:
+ Ron=100 Roff=38K R0=30K D=10N uv=10F ith1=0 ith0=0
      ********** Differential equation modeling ***********
Gx 0 x value={I(Emem)*uv*Ron/D^2*f(V(x),I(Emem),c1,c2,g1,g2)}
Cx x 0 1 IC={(Roff-R0)/(Roff-Ron)}
Raux x 0 1T
*********** Memristance ************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
*********** Flux computation**********************
Eflux flux 0 value={SDT(V(plus, minus))}
************************************************
*********** Charge computation*********************
Echarge charge 0 value={SDT(I(Emem))}
*********** PWL window function *****************
.func f(x,i,c1,c2,g1,g2)={stp(i-ith1)*f1(x,c1,c2,g1)+stp(-i-
ith0)*f2(x,c1,c2,g2)}
************** f1 *******************************
.func f1(x,c1,c2,g1)={IF(x<0,0,IF(x<c1,(1-g1)/c1*x+g1,
+IF(x<=c2,1,IF(x<=1,1/(c2-1)*x-1/(c2-1),0)))))}
************** f2 *******************************
.func f2(x,c1,c2,g2)={IF(x<0,0,IF(x<c1,1/c1*x,
+IF(x<=c2,1,IF(x<=1,(g2-1)/(1-c2)*x+(1-g2*c2)/(1-c2),0)))))}
.ENDS HMemristor
```

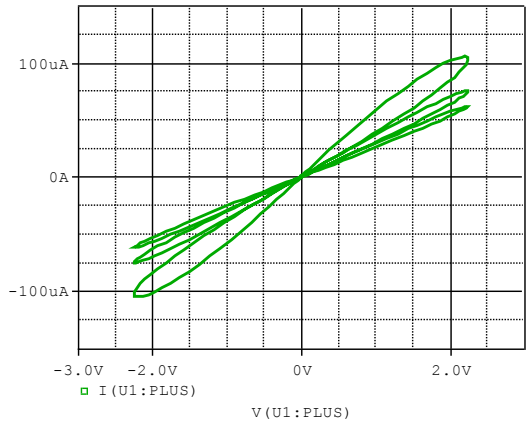

Fig. 6. Simulation of the built SPICE memristor model

V. A MEMRISTOR-BASED SMALL-WORLD NEURAL NETWORK

A. Description of Small-world Multilayer Network

Designing a small-world multilayer neural network begins with a regular multilayer feed-forward network where the neurons in one layer connect every neuron in its adjacent layers. Then, by randomly breaking one original link each time with a predefined probability, and freely picking up a new neuron from the subsequently nonadjacent layers, a new cross-layer link is built. Repeat this rewiring operation till all the original links have been considered once, and finally one can get a small-world model with a majority of local connections and some long-distance global connections. Fig. 7 shows a diagram of a multilayer feed-forward neural network, where some short connections in the original regular network are cut off (dashed lines), then an equal amount of long connections are generated (red solid lines), leading to a small-world multilayer network model.

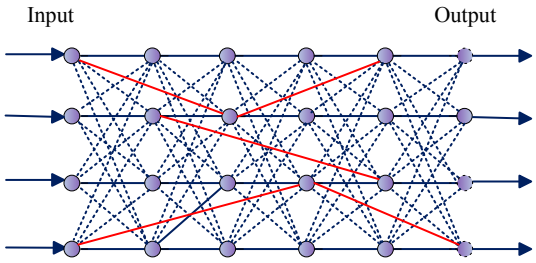

Fig.7. Small-world multilayer neural network

More specially, we set the network connection matrix as W, and W^l (l=1,2,3...5) denotes the connection sub-matrix between the lth layer and the $(l+1)$th layer. Hence, the connection matrix of the original regular network W can be written as

$$W = \begin{pmatrix} 0 & W^1 & 0 & 0 & 0 & 0 \\ 0 & 0 & W^2 & 0 & 0 & 0 \\ 0 & 0 & 0 & W^3 & 0 & 0 \\ 0 & 0 & 0 & 0 & W^4 & 0 \\ 0 & 0 & 0 & 0 & 0 & W^5 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}, \quad (11)$$

in which a zero means no connection exists between the corresponding layers. After the rewiring operation, the connection matrix of the resulting small-world multilayer network can be got as

$$W' = \begin{pmatrix} 0 & W^{1'} & E_1^3 & E_1^4 & E_1^5 & E_1^6 \\ 0 & 0 & W^{2'} & E_2^4 & E_2^5 & E_2^6 \\ 0 & 0 & 0 & W^{3'} & E_3^5 & E_3^6 \\ 0 & 0 & 0 & 0 & W^{4'} & E_4^6 \\ 0 & 0 & 0 & 0 & 0 & W^{5'} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}, \quad (12)$$

where $W^{l'}$ represents the reconnection sub-matrix between the lth layer and the $(l+1)$th layer, and $E_l^{l'}$ represents the sub-matrix between two nonadjacent layers, with $l \in \{1,2,3,4\}, l' \in \{3,4,\cdots$.

B. Synaptic Connection Implementation Based on the PWL Memristor

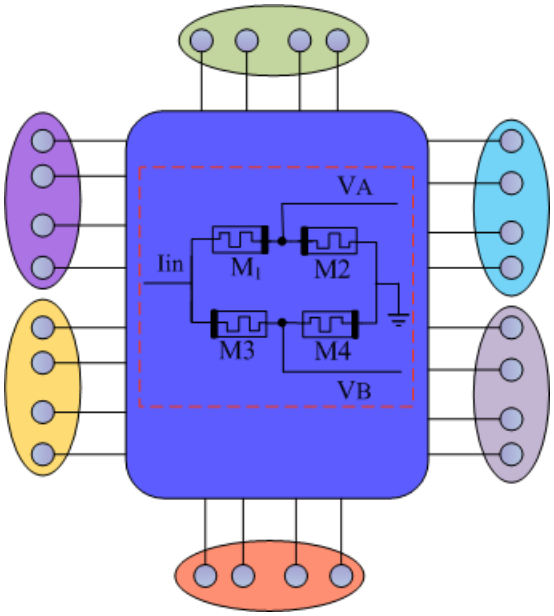

Fig.8. Block diagram of a small-world neural network with memristor bridge circuits.

The small-world model was proposed for the purpose of more practically reflecting a real brain neural network. Better software performance, e.g., faster learning or convergence speed, has been the research focus [18]. However, the

corresponding physical implementation has not been discussed in literature. That is mainly because of the fact that the small-world network model cannot reduce the total number of connections. Thus, by using traditional hardware realization schemes for synaptic circuits, the small-world neural network also faces the scalability problem like other neural network models. This situation actually hinders its potential applications in practice. Fortunately, the emerging memristor in nanoscale structure may provide an opportunity for the analog implementation of the small-world neural networks.

Fig.8 shows a block diagram of small-world neural networks with memristor-based synaptic circuits. The surrounding ellipses represent several neuron layers and all of the synapses are contained in the round corner rectangle. In this study, we propose to use the PWL memristor in a bridge architecture to realize the electric synapse inspired by [19]. Such a synapse is presented in the center rectangle which takes charge of weight programming and weighting operations. It is consisted of four identical PWL memristors (denoted by M_1, M_2, M_3, and M_4). Assume that the signal from the presynaptic neuron is I_{in} (positive or negative), through a memristor-based synaptic circuit, the output voltage between is calculated by

$$V_{AB} = \left(\frac{M_2}{M_1 + M_2} - \frac{M_4}{M_3 + M_4}\right) \cdot I_{in}, \qquad (13)$$

and then transmitted to a postsynaptic neuron. If $M_2 / M_1 > M_4 / M_3$, the synaptic weight is positive, if $M_2 / M_1 < M_4 / M_3$, the synaptic weight is negative, and if $M_2 / M_1 = M_4 / M_3$, there is a zero weight. The capability of realizing these three types of weights by using only one synaptic circuit makes it a promising candidate for electric synapse. Set $R_L = 100\Omega$ and $R_H = 20k\Omega$, the multiplication factor obtained from the synaptic circuit falls in [-0.99 0.99]. More detailed description can be found in our extended paper [20].

During weight-setting and weight-updating procedure, a big programming current is applied to set these memristors into corresponding resistance states. While weighting processing, the signal to be weighted is converted into a proper input excitation smaller than the threshold of the memristor. So it would not change the set memristance accidentally. In the following experiments, we set the threshold as 0.5 mA.

Note that, as shown in Fig.8, the memristor-based synaptic circuit units are originally built up and connected with neurons. The forming of small-world multilayer networks rewire some connections, i.e., reconnecting a presynaptic neuron's output from a postsynaptic neuron to another. But the new connection is still realized through the same synaptic unit as the original one. Therefore, the rewiring does not change the total number of connections and would not bring scaling problem.

C. Small-world Multiplayer Neural Network for Function Approximation

One of the important applications of a feed-forward multilayer neural network is nonlinear function approximation. Here, the function to be approximated is given by

$$f(x) = 0.4 \times \sin(\pi x) + 0.1 \times \sin(10\pi x) + 0.7. \qquad (14)$$

Since there are several local minimums, the network is supposed to have qualified ability to get out of the local minimums to achieve satisfactory approximation results.

The neural network under investigation is constituted by seven layers with one neuron in the input layer, one in the output layer, and five in each of the five hidden layers. The activation function of the neurons is Sigmoid function. By applying the generating principle described in Section V-B to all original local connections except the last hidden layer and the output layer with a predefined rewiring probability *p*, we get a neural network with small-world topology.

The memristor synaptic weight is set and updated based on the BP learning rule while training procedure. The weight modification between the neuron *j* in the (*l-1)*th layer and the neuron *i* in the *l*th layer is determined by

$$\Delta w_{ij}(l) = \alpha w_{ij}(l-1) - \eta \cdot \delta_j O_i, \qquad (15)$$

where α is the learning rate, η is the momentum factor, O_i is output of the neuron *i*. δ_j, the local gradient of the neuron *j* in the *l*th layer, is calculated for the output layer and the others in different ways, which is expressed by

$$\delta_j = \begin{cases} -(T_j - O_j) O_j (1 - O_j) \\ O_j (1 - O_j) \sum_i w_{ji} \delta_i \end{cases}. \qquad (16)$$

The top portion of (16) is for the output layer, and the bottom one is used for the other layers. And T_j denotes the target value.

In order to verify the superior performance of the small-world neuronal networks and figure out the optimal structure, we conducted a series of simulations on Matlab by setting $\alpha = 0.95$, $\eta = 0.25$, and initial weighs as random values falls in [-0.5 0.5]. Fig.9 shows the approximation speed (iteration times) of different network structures, i.e., the smallest iteration number for reaching the predefined approximation error 0.0001. Each drawn point is the average value of 100 times runs. It can be observed that the small-world networks (0<p<1) need much less iteration times than the regular neural network (when p=0), which demonstrates its advantage in processing speed. Furthermore, when $p = 0.1$, the network has the fast approximation speed.

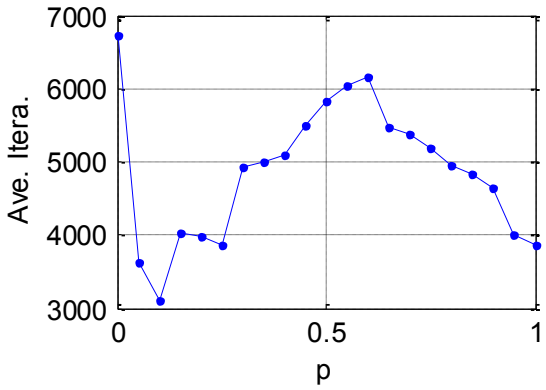

Fig. 9. The relationship between iteration and rewiring probability.

Let the maximum allowable iteration times be 10,000, as previously mentioned for each p, we performed the simulation for 100 times, where the effective approximation times, i.e. error < 0.0001 within 10,000 iterations, is presented in Fig.10. It can be found that the small-world networks have higher accuracy rate than the regular network. A satisfactory approximation result with $p = 0.1$ is shown in Fig.11 in which every drawn point is a mean value of 100 times repeated simulations. Therefore, the effectiveness of the proposed small-world network is thus verified.

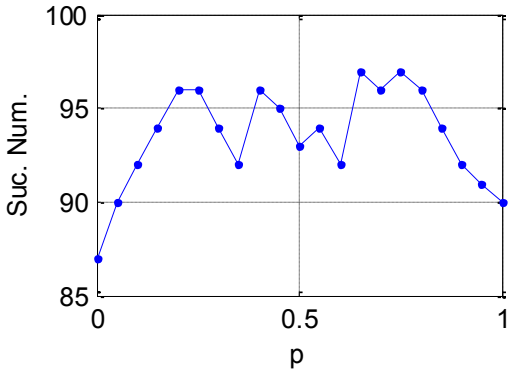

Fig. 10. The effective approximation number in 100 times simulations under varying rewiring probability.

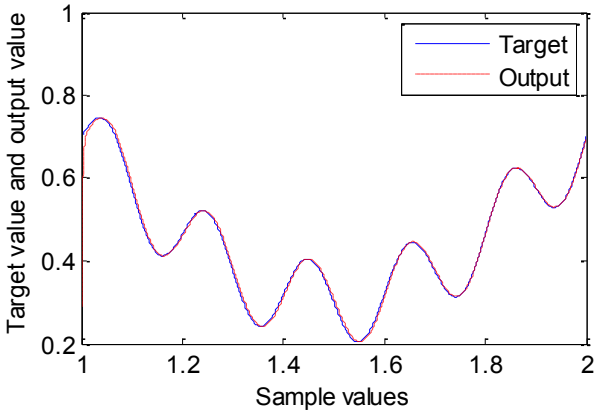

Fig.11. Simulation for function approximation, $p = 0.1$.

VI. CONCLUSION

This paper presents a novel mathematical model of the HP memristor by designing a PWL window function with four tunable parameters. This model: (a) can represent all of the other compared models by adjusting the parameters; (b) It can reflect the most practical behaviors among the compared models and avoid serious issues like in linear and Joglekar model; (c) It considers the thresholds, which is not found in the other models, but is significance for practical applications. Numerical simulations and comparisons validate the accuracy and demonstrate advantages of the proposed model. In the second part, a new kind of small-world neural network using the proposed memristor in a bridge circuit as synaptic circuits is proposed. Simulation results for a nonlinear function approximation verify the superior performance of small-world networks over the original regular neural networks in approximation speed and effect, as well as indicate the effectiveness of the proposed scheme.

This work may provide a reference to physically realize the small-world neural networks and promote the development of neuromorphic computing. Future work will include refining the model when more experimental data is available. More effects will be devoted to the investigation of the memristor-based small-world networks, including the rewiring strategy improvement, the rewiring probability selection, and the topology design.

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