# **Robust Doublet STDP in a Floating-Gate Synapse**

Roshan Gopalakrishnan\* and Arindam Basu<sup>†</sup>

School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore Email: \*roshan005@e.ntu.edu.sg;<sup>†</sup>arindam.basu@ntu.edu.sg

Abstract—Learning in a neural network typically happens with the modification or plasticity of synaptic weight. Thus the plasticity rule which modifies the synaptic strength based on the timing difference between the pre- and post-synaptic spike occurrence is termed as Spike Time Dependent Plasticity (STDP). This paper describes the neuromorphic VLSI implementation of a synapse utilizing a single floating-gate (FG) transistor that can be used to store a weight in a nonvolatile manner and demonstrate biological learning rules such as Long-Term Potentiation (LTP), Long-Term Depression (LTD) and STDP. The experimental STDP plot of a FG synapse (change in weight against  $\Delta t = t_{post} - t_{pre}$ ) from previous studies shows a depression instead of potentiation at some range of positive values of  $\Delta t$  for a wide set of parameters. In this paper, we present a simple solution based on changing control gate waveforms of the FG device that makes the weight change conform closely with biological observations over a wide range of parameters. We show results from a theoretical model to illustrate the effects of the modified waveform. The experimental results from a FG synapse fabricated in AMS 0.35µm CMOS process design are also presented to justify the claim.

#### I. INTRODUCTION

Over the last decade, numerous experimental studies [1], [2] have shown that the synaptic strength modifies as a function of the spike timing difference  $\Delta t = t_{post} - t_{pre}$  between the firing times  $t_{pre}$  and  $t_{post}$  of the presynaptic and postsynaptic neurons respectively. This phenomenon, called Spike Time-Dependent Plasticity (STDP), has emerged as one of several unsupervised plasticity rules that play an important role in learning and memory in the brain. The STDP based on a pair of pre- and post-synaptic spike is referred as doublet STDP (D-STDP) while the one based on triplet of synaptic spikes i.e either pre-post-pre synaptic spike or post-pre-post synaptic spike is referred as triplet STDP (T-STDP). In this paper we deal only with D-STDP and henceforth, we will imply the doublet rule when we mention STDP. The STDP model employs two phenomenon: one is long term potentiation (LTP) which is elicited by increase in synaptic weight due to the occurrence of postsynaptic spike after a presynaptic spike whereas the second one is long term depression (LTD) in which the synaptic weight is reduced when the timing relation is reversed.

Due to the popularity of STDP in computational neuroscience, neuromorphic engineers who aim to emulate brain function using VLSI have also tried to emulate this behaviour in silicon. However, implementing a compact learning synapse remains one of the big challenges in the field. Several recent papers have reported STDP implementations [4], [5]; however,



Fig. 1: Floating gate Mosfet : The different terminal voltages  $V_{tun}$ ,  $V_g$ ,  $V_d$  as shown above are used to obtain the desired plasticity rule. The gate voltage waveform,  $V_g$  shown in black is the original voltage waveform which is as in [3] and the gate voltage waveform,  $V_g$  in red dashed line is the novel modified technique.

these synapses could only hold two states in long term. The size of these synapses are also large hindering scalability of these designs. A promising solution for non-volatile analog weight storage is provided by a floating-gate (FG) device which is typically used to implement flash memory. This concept was utilized recently to show weight storage and adaptation due to quantum mechanical processes based on input signal timing [3]. Since then, it has also been used in a reconfigurable neural network as well [6]. However, the experimental result of STDP using FG (Fig. 7(a) in [3]) in [3] has a difference when compared to biological findings: the FG synapse shows depression instead of potentiation for some range of positive  $\Delta t$ .

To ameliorate the STDP graph of a FG synapse obtained in [3], a minimum hardware overhead solution is proposed in this paper. The solution contains a modified gate voltage waveform in red dashed line as shown in Fig. 1 while the gate voltage waveform proposed in previous work [3] is shown in black line in the same figure. The paper is organized as follows: Section II provides a brief explanation of STDP model. Section III-A introduces the working of floating gate synapse. To vindicate the novelty proposed in the paper, a mathematical model of the



Fig. 2: Theoretical implementation of Doublet STDP (D-STDP): The plot is based on equation 1 with the parameters  $A^+ = 4.6$ m and  $A^- = 3$ m.

weight update is presented in III-B. The experimental results and its discussion are included in section IV. Finally the paper is ended with conclusion of the work.

#### **II. STDP SYNAPTIC MODIFICATION RULE**

An essential requirement for learning in real and artificial neural networks is synaptic modification. In biology, synapses are specialized structures to permit the conductivity of chemical or electrical signals between two neurons with an associated synaptic strength or weight. Learning typically implies the modification of synaptic weight due to the activities of the pre- and post-synaptic neurons. There are two types of synaptic weight change: one is potentiation or increase of weight while the other is depression or reduction in weight. In case of STDP, these two modifications are based on the timing of pre- and post-synaptic spikes as described next.

## A. Doublet STDP

In doublet STDP, potentiation occurs when a postsynaptic spike succeeds a presynaptic spike; otherwise depression happens. The weight changes can be governed by a temporal learning window. The temporal learning window for STDP can be expressed as [7], [8]

$$\Delta w = \begin{cases} \Delta w^+ = A^+ e^{\left(\frac{-\Delta t}{\tau_+}\right)} & \text{if } \Delta t \ge 0\\ \Delta w^- = -A^- e^{\left(\frac{\Delta t}{\tau_-}\right)} & \text{if } \Delta t < 0 \end{cases}$$
(1)

where  $\Delta t = t_{post} - t_{pre}$  is the time difference between a post-synaptic and pre-synaptic spike,  $\tau_+$  and  $\tau_-$  are the time constants of the learning window, and  $A^+$  and  $A^-$  are the maximal weight changes for potentiation and depression, respectively. The theoretical graph for the above equation is simulated using MATLAB and is shown in Fig. 2 with the parameters being obtained by data fitting as explained in [8]. As mentioned by Bi and Poo in [9],  $\tau_+$  and  $\tau_-$  are taken as 16.8ms and 33.7ms respectively for the simulation.

#### **III. FLOATING GATE SYNAPSE**

## A. BASIC OPERATION

The equation for drain current of a subthreshold saturated pFET whose well is tied to  $V_{dd}$  is given by [3]

$$I_d = I_{s0} e^{\kappa (V_{dd} - V_{fg})/U_T} \tag{2}$$



Fig. 3: Parameter specifications of terminal voltage waveforms : The different parameters are given as  $T_g = 34$ ms,  $T_{tun} = 300$ ms,  $T_d = 300$ us,  $V_{tun\_max} = 12$ V,  $V_{tun\_min} = 5.6$ V,  $V_{g\_max} = 3.3$ V,  $V_{g\_min} = 2.5$ V,  $V_{d\_max} = 5$ V and  $V_{d\_min} = 0$ V.

where  $U_T$  is the thermal voltage and  $\kappa$  is the gate coupling coefficient. Due to the exponential relationship between the gate voltage and drain current of the MOS transistor, the gating voltage to the synapse has to be a triangular waveform which decreases from its maximum value [3]. The current at the maximum gate voltage is nearly zero. In order to generate EPSCs similar to biological observations, we apply triangular waveform with unequal slopes at the input [3]. The fast decreasing part of the input triangular waveform with slope  $S_1$ results in a quick rise of the synaptic current while the slowly increasing part with slope  $S_2$  determines the exponential decay in the output current. In this paper we modify the triangular waveform present at the input without harming the generation of EPSCs similar to biological observation.

The synaptic weight adaptation for obtaining different plasticity rule depends on the signals on the FG mosfet. The terminal voltages of the floating gate transistor shown in the Fig. 1 are the gate voltage  $V_g$ , drain voltage  $V_d$  and tunneling voltage  $V_{tun}$ . The specifications of terminal voltage waveforms are given in Fig. 3.

Synaptic weight modification in a FG mosfet uses a combination of hot-electron injection (HEI) and Fowler-Nordheim tunneling [3]. HEI adds electrons on to the floating gate node, which reduces the voltage on the floating gate thus resulting in more current through the transistor hence increasing the weight of the synapse. On the other hand tunneling takes away electrons from the FG node, which increases the voltage of floating gate node thus reducing the drain current of the transistor and the synaptic weight. At every pre-synaptic spike, a triangular gate voltage waveform is generated while at every post-synaptic spike, a triangular tunneling voltage and a drain voltage pulse is generated as illustrated in the Fig. 4(a) and (b). Hence, injection and tunneling currents (and the resultant weight change) also depend on the time difference between pre- and post-synaptic spike times. The governing equations for injection and tunneling are given as [10], [3]

$$I_{inj} = I_{inj0} (I_d/I_{s0})^{\alpha} e^{-\Delta V_{ds}/V_{inj}}$$

$$I_{tun} = I_{tun0} e^{(V_{tun} - V_{fg})/V_{ox}}$$
(3)

where  $I_d$  is the drain current,  $\alpha = 1 - U_T/V_{inj}$ ,  $V_{ox}$  and  $V_{inj}$  are process dependent parameters.



Fig. 4: Timing diagram for STDP in FG synapse. (a) The plot shows the time instances of pre- and post- synaptic spike occurrence for the case of  $\Delta t = (t_{post} - t_{pre}) > 0$ . Note the timescale which helps while integration during +ve  $\Delta t$  of the STDP curve. (b) The plot shows the time instances of pre- and post- synaptic spike occurrence for the case of  $\Delta t = (t_{post} - t_{pre}) < 0$ . Note the timescale which helps while integration during -ve  $\Delta t$  of the STDP curve.

### B. THEORETICAL MODEL OF LEARNING

If we compare the result obtained from the experimental measurement using original gate voltage waveform in Fig. 7(a) of [3] with the theoretical graph of STDP in Fig. 2, we notice that there is depression happening instead of potentiation on the positive x-axis of the experimental curve of STDP. To understand this effect, we first develop a mathematical model of the change in weight for a FG synapse. The weight of the synaptic device is defined as [3]:

$$w = e^{\frac{-\kappa V_{fg}}{U_T}} \tag{4}$$

Hence, equations to predict the change in FG voltage effectively predict the change in weight. The following assumptions are made in deriving the theoretical equations:

1) To ensure small change in weight at very large negative and positive values of  $\Delta t$ ,  $V_{g\_init}$  has to be high enough so that  $V_{tun\_max}$  -  $V_{g\_init}$  is small enough for negligible tunneling. Similarly  $\Delta V_g = V_{g\_init}$  -  $V_{g\_min}$ , should be small enough so that  $V_{tun\_init}$  -  $V_{g\_min}$  is small enough for negligible tunneling.

2) Strong coupling from gate to floating gate node where as a weak coupling from tunneling node to floating gate node. This is justified since typically  $C_g >> C_{tun}$ .

3) The gate voltage waveform falls to its minimum value instantaneously. In other words,  $S_1 >> S_2$ ,  $S_3$  as shown in Fig. 3. Also, we use  $T_g$  to denote the temporal duration of gate voltage with the understanding that  $T_g = T_{g\_ori}$  for the original waveform proposed in [3] while  $T_g = T_{g\_mod}$  for our

proposed modification.

We can now derive the slow time scale equation [3] for change in FG voltage due to tunneling and injection as:

$$C_T \frac{d\overline{V_{fg}}}{dt} = I_{tun} - I_{inj} = C_T \frac{d\overline{V_{fg2}}}{dt} - C_T \frac{d\overline{V_{fg1}}}{dt}$$
(5)

where  $C_T$  is the total capacitance on the FG node and  $\overline{V_{fg}}$  denotes change on a slow time scale.

1) Case 1:  $\Delta t > 0$ : First, we consider the case of  $\Delta t > 0$ i.e the positive axis of STDP curve and combine equations (3) and (2) to get:

$$C_T \frac{\overline{dV_{fg1}}}{dt} = -I_{inj0} (e^{\kappa (V_{dd} - V_{fg})/U_T})^{\alpha} e^{-\Delta V_{ds}/V_{inj}}$$
(6)

where  $\overline{V_{fg1}}$  is the slow time scale change in  $V_{fg}$  due to injection only. Since change in  $V_{fg}$  on the RHS happens due to coupling from the gate voltage, we can write:

$$V_{fg} = V_{fg\_min} + \frac{C_g}{C_T} S_2 t \tag{7}$$

where  $S_2$  is positive slope of  $V_g$  and  $C_g$  is the capacitance connected between the gate terminal and the floating gate terminal. Here  $V_{fg\_min}$  is not same as  $V_{g\_min}$  due to initial charge stored on the FG. Substituting equations (7) in equation (6),we get

$$C_T \frac{\overline{dV_{fg1}}}{dt} = -Ae^{-Xt} \tag{8}$$



Fig. 5: Weight variation in FG synapse obtained from theory for the two different gate voltage waveforms. (a) shows the effect of injection on  $\Delta V_{fg}$  for the case  $\Delta t = (t_{post} - t_{pre}) > 0$ , (b) shows the effect of tunneling on  $\Delta V_{fg}$  for the case  $\Delta t = (t_{post} - t_{pre}) > 0$ , (c) shows the effect of tunneling on  $\Delta V_{fg}$  for the case  $\Delta t = (t_{post} - t_{pre}) > 0$ , (c) shows the effect of tunneling on  $\Delta V_{fg}$  for the case  $\Delta t = (t_{post} - t_{pre}) < 0$ , (d) shows the effect of both injection and tunneling on  $\Delta w/w$  which is equivalent to  $\Delta V_{fg}$ . (e) shows the result as in (d) but for a different parameter of  $V_{tun\_max} = 11$  V while (f) shows the result for  $V_{tun\_max} = 11$  V but  $\Delta V_d = 4.5$  V.

where

$$A = I_{inj0} e^{\alpha \kappa (V_{dd} - V_{fg\text{-}min})/U_T} e^{-\Delta V_{ds}/V_{inj}}$$

$$X = \frac{\alpha \kappa C_g S_2}{C_T U_T}$$
(9)

Referring to Fig. 4(a), significant amount of injection happens in the time from  $\Delta t$  to  $\Delta t + T_d$ , where  $\Delta V_{ds}$  is constant and significant. Also, since  $T_d$  is very small compared to  $T_g$ , we can assume that  $V_g$  is constant during the drain pulse. Hence, we finally get:

$$C_T \Delta \overline{V_{fg1}} = -AT_d e^{-X\Delta t} \tag{10}$$

The above equation for  $\Delta \overline{V_{fg}}$  is a function of  $\Delta t$  and is shown in Fig. 5(a) (plotted in red and marked as "Original  $V_g$ ").

Now let us analyze the contribution of tunneling to  $\Delta \overline{V_{fg}}$  denoted as  $\Delta \overline{V_{fg2}}$ . With reference to Fig. 4(a) and from assumption 1, the effect of tunneling is significant only from  $\Delta t$  to  $T_g$ . Hence, we have:

$$C_T \int_0^{\Delta \overline{V_{fg2}}} \overline{dV_{fg}} = \int_{\Delta t}^{T_g} I_{tun} dt \tag{11}$$

Substituting  $I_{tun}$  from equation (3), we further get:

$$C_T \Delta \overline{V_{fg2}} = \int_{\Delta t}^{T_g} I_{tun0} e^{(V_{tun} - V_{fg})/V_{ox}} dt \qquad (12)$$

where

$$V_{tun} = \begin{cases} V_{tun\_init} & if \quad 0 < t < \Delta t \\ V_{tun\_max} + S_3(t - \Delta t) & if \quad \Delta t < t < T_g \end{cases}$$
(13)

where  $S_3$  is the negative slope of  $V_{tun}$ . Thus substituting equations (13) and (7) into (12), we finally get:

$$C_T \Delta \overline{V_{fg2}} = B e^{\frac{-S_2 \Delta t}{V_{ox}}} \int_{\Delta t}^{T_g} e^{Yt} dt$$

$$= B' (e^{YT_g} - e^{Y\Delta t}) e^{\frac{-S_2 \Delta t}{V_{ox}}}$$
(14)

where

$$Y = \frac{S_3 - \frac{C_g S_2}{C_T}}{V_{ox}}$$

$$B = I_{tun0} e^{\frac{V_{tun,max} - V_{fg,min}}{V_{ox}}}$$

$$B' = B/Y$$
(15)

 $A^+$  is obtained from the sum of  $\Delta \overline{V_{fg1}}$  and  $\Delta \overline{V_{fg2}}$  at  $\Delta t =$ 

0 (ideal case). Hence we get,

$$A^{+} = \frac{-k\Delta\overline{V_{fg}}|_{\Delta t=0}}{U_{T}}$$
$$= \frac{-k(\Delta\overline{V_{fg1}} + \Delta\overline{V_{fg2}})|_{\Delta t=0}}{U_{T}}$$
$$= \frac{-k(-AT_{d} + B'(e^{YT_{g}} - 1))}{C_{T}U_{T}}$$
(16)

From this we can conclude that  $A^+$  depends on free parameters  $\Delta V_{ds}$  and  $V_{tun_max}$ . Similarly  $\tau^+$  can be calculated from the equation  $\frac{-k\Delta V_{fg}}{U_T} = 0.1\% of A^+$ .  $\Delta t$  obtained after solving the equation gives the value of  $\tau^+$ . Intuitively we could see that  $\tau^+$  depends mainly on  $T_g$ . The above equation for  $\Delta \overline{V_{fg}}$  is also a function of  $\Delta t$  and

is shown in Fig. 5(b).

2) Case 2:  $\Delta t < 0$ : Now we consider the case of  $\Delta t =$  $(t_{post} - t_{pre}) < 0$  i.e the negative axis of STDP curve. Similar to what we have done above, let us see the effect of tunneling and injection separately.

For the contribution of injection to  $\overline{V_{fg}}$ , we could see that injection happens only during the initial small period,  $T_d$  of time axis where the drain current of the MOS is almost zero. So we can completely neglect the effect of injection on  $V_{fg}$ in this case.

Now let us consider the contribution of tunneling to  $\overline{V_{fg}}$ . Similar to the analysis above, using assumption 1, we have:

$$C_T \int_0^{\Delta \overline{V_{fg2}}} dV_{fg} = \int_{-\Delta t}^{T_{tun}} I_{tun} dt$$
(17)

While performing the integration, there arises two cases for the upper limit of integration based on whether  $-\Delta t + T_q$  is greater or lesser than  $T_{tun}$ . Also, similar to the case of positive  $\Delta t$ , here we have:

$$V_{fg} = V_{fg\_min} + \frac{C_g}{C_T} S_2(t - (-\Delta t))$$

$$V_{tun} = V_{tun\_max} + S_3 t$$
(18)

Substituting equations (18) and (3) into equation (17), we get case 1:  $-\Delta t + T_g < T_{tun}$ 

$$C_T \Delta \overline{V_{fg2}} = B e^{\frac{-C_g S_2 \Delta t}{C_T V_{ox}}} \int_{-\Delta t}^{-\Delta t + T_g} e^{Yt} dt$$

$$= B' (e^{Y(T_g - \Delta t)} - e^{-Y\Delta t}) e^{\frac{-C_g S_2 \Delta t}{C_T V_{ox}}}$$
(19)

case 2:  $-\Delta t + T_g > T_{tun}$ 

$$C_T \Delta \overline{V_{fg2}} = B e^{\frac{-C_g S_2 \Delta t}{C_T V_{ox}}} \int_{-\Delta t}^{T_{tun}} e^{Yt} dt$$

$$= B' (e^{YT_{tun}} - e^{-Y\Delta t}) e^{\frac{-C_g S_2 \Delta t}{C_T V_{ox}}}$$
(20)

where Y, B and B' are as given above.

Here  $A^-$  is obtained from  $\Delta \overline{V_{fg}}$  at  $\Delta t = 0$  (ideal case). Hence we get,

case 1:  $-\Delta t + T_g < T_{tun}$ 

$$A^{-} = \frac{-k\Delta\overline{V_{fg}}|_{\Delta t=0}}{U_{T}}$$
$$= \frac{-k(B'(e^{YT_{g}} - 1))}{C_{T}U_{T}}$$
(21)

case 2: 
$$-\Delta t + T_g > T_{tun}$$
  

$$A^- = \frac{-k\Delta \overline{V_{fg}}|_{\Delta t=0}}{U_T}$$

$$= \frac{-k(B'(e^{YT_{tun}} - 1))}{C_T U_T}$$
(22)

From this we can conclude that  $A^-$  depends on free parameters  $T_{tun}$  and  $V_{tun_max}$ . Similarly  $\tau^-$  can be calculated from the equation  $\frac{-k\Delta V_{fg}}{U_T} = 0.1\% \text{ of } A^-$ .  $\Delta t$  obtained after solving the equation gives the value of  $\tau^-$ . Intuitively we could see that  $\tau^-$  depends mainly on  $T_{tun}$ .

The above equation for  $\Delta \overline{V_{fg}}$  is a function of  $\Delta t$  which can be plotted on the graph and is shown in Fig. 5(c). Both original and modified cases of gate voltage waveform is plotted in the figure. The combined effect of tunneling and injection is shown in Fig. 5(d). It is clearly seen that the theoretical model does predict a depression of weight for some range of positive values of  $\Delta t$ . Next, we shall analyze the reason behind this and suggest a method to rectify this.

#### C. Proposed STDP protocol for FG synapse

Since we want there to be only potentiation for positive values of  $\Delta t$ , we have to design the parameters of the FG synapse so that injection dominates over tunneling in this entire range. On the other hand, we want tunneling to dominate over injection for all negative values of  $\Delta t$ . From Fig. 5(d) we see that for a range of positive values of  $\Delta t$ , tunneling dominates over injection. The reason for this can be realized by studying the injection and tunneling characteristics separately in Fig. 5(a) and (b) respectively. We can see that the effect of injection reduces to zero at  $\Delta t \approx 10$  ms (Fig. 5(a)) while the effect of tunneling persists till  $\approx 30$  ms (Fig. 5(b)). This results in tunneling dominating for  $\Delta t > \approx 10$  ms creating depression.

The reason for the sharp decline of the potentiation curve in Fig. 5(a) is that injection depends directly on drain current which reduces exponentially fast with  $\Delta t$  (equation 10). Thus there is a large part of the gate waveform (the part for which  $V_g > \approx V_{g\_min} + 0.2$  V) which does not create significant postsynaptic current or potentiation. Intuitively, we can eliminate this part and get a modified gate control voltage waveform as shown in Fig. 4. The effect of this modification on the weight change curve is shown in Fig. 5(d) (blue curve marked "modified  $V_g$ "). As predicted, the magnitude of depression for positive values of  $\Delta t$  is much reduced now. For certain sets of parameters (e.g. if  $V_{tun_max}$  is much lower or  $V_{g_min}$  is higher), the original gate waveform also does not produce significant depression for  $\Delta t > 0$ . As an example, Fig. 5(e) plots the STDP curve for parameter,  $V_{tun\_max} = 11$  V



Fig. 6: Experimental results of floating gate device: (a) the experimental result of STDP with original gate voltage waveform. Similarly (b) the experimental result of STDP with modified gate voltage waveform.

showing no appreciable depression for positive  $\Delta t$ . However, the modified waveform provides a more bio-realistic STDP curve for a much wider set of parameters and hence is more robust. As an example, Fig. 5(f) plots the STDP curve with  $V_{tun\_max} = 11$  V but with a reduced  $\Delta V_d = 4.5$  V compared to  $\Delta V_d = 5$  V in the earlier case. It can be seen that the original gate voltage waveform again creates a depression while the proposed one is free from this artifact.

## IV. EXPERIMENTAL RESULTS

The floating gate synapse, from which the experimental measurements are obtained, was designed in AMS  $0.35\mu$ m CMOS process. The gate voltage waveform shown has two cases as discussed in the earlier section. The experimental results of both the cases of gate voltage waveform is given in Fig. 6.

Figure 6(a) plot the case of STDP for the original gate waveform described in [3]. It does show the case of depression for some range of positive values of  $\Delta t$ . The similar plot for

the case of modified gate waveform is shown in Fig. 6(b). Indeed, the new proposed gate waveform is able to remove the undesired effect in Fig. 6(a) thus validating the theoretical analysis.

## V. CONCLUSION

We have presented a robust STDP rule using single FG transistor acting as a learning synapse for VLSI spiking neural networks. Compared to earlier work in [3], our proposed method allows the STDP curve of the FG device to be similar to the biological one over a much wider range of parameters. This is achieved by simply modifying the gate voltage waveform-hence, the hardware overhead compared to [3] is minimal. A mathematical model for learning is presented to illustrate the benefit of our proposed method. We also present measurement results from a  $0.35\mu m$  chip to justify the claim.

## VI. ACKNOWLEDGEMENT

Financial support from MOE AcRF grant RG21/10 is acknowledged.

#### REFERENCES

- L. F. Abbott and S. B. Nelson, "Synaptic plasticity: taming the beast," *Nature neuroscience*, vol. 3, pp. 1178–1183, November 2000.
- [2] J.-P. Pfister, *Theory of Non-Linear Spike-Time Dependent Plasticity*, Ph.D. thesis, Swiss Federal Institute of Technology, Lausanne, Switzerland, 2006.
- [3] S. Ramakrishnan, P. Hasler, and C. Gordon., "Floating gate synapses with spike-time-dependent plasticity," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, June 2011.
- [4] J. Arthur and K. Boahen, "Synchrony in silicon: The gamma rhythm," *IEEE Transactions on Neural Networks*, vol. 18, no. 6, pp. 1815–1825, Nov 2007.
- [5] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI Array of Low-Power Spiking Neurons and Bistable Synapses With Spike-Timing Dependent Plasticity," *IEEE Transactions on Neural Networks*, vol. 17, no. 1, pp. 211–221, Jan 2006.
- [6] S. Brink, S. Nease, P. Hasler, S. Ramakrishnan, R. Wunderlich, A. Basu, and B. Degnan, "A learning-enabled neuron array IC based upon transistor channel models of biological phenomenon," *IEEE Transactions* on Biomedical Circuits and Systems, vol. 7, no. 1, pp. 71–81, Feb 2013.
- [7] M. R. Azghadi, O. Kavehei, S. Al-Sarawi, N. Iannella, and D. Abbott, "Novel VLSI implementation for triplet-based spike-timing dependent plasticity," in *ISSNIP*, 2011.
- [8] J.-P. Pfister and W. Gerstner, "Triplets of spikes in a model of spike timing-dependent plasticity," *The Journal of Neuroscience*, pp. 9673– 9682, September 2006.
- [9] G.-Q. Bi and M.-M. Poo, "Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type," *The Journal of Neuroscience*, vol. 18, pp. 10464– 10472, 1998.
- [10] P. Hasler, A. Basu, and S. Koziol, "Above threshold pfet injection modeling intended for programming floating-gate systems," *ISCAS*, pp. 1557–1560, May 2007.