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Implementation of Memristive Neural Networks with Spike-rate-dependent Plasticity Synapses

Yide Zhang, Zhigang Zeng and Shiping Wen

Abstract— **The property of changing resistance according to applied currents of memristors makes them candidates for emulating synapses in artificial neural networks. In this paper, we introduce a memristive synapse design into neural network circuits. Combined with modified integrate-and-fire (I&F) complementary metal-oxide-semiconducter (CMOS) neurons, the memristive neural network shows similarities to its biological counterpart, in respect of biologically realistic, current-controlled spikes and adaptive synaptic plasticity. Then, the spike-rate-dependent plasticity (SRDP) of the synapse, an extended protocol of the Hebbian learning rule, is originally implemented by the circuit. And some advanced neural activities including learning, associative memory and forgetting are realized based on the SRDP rule. These activities are comprehensively validated on a neural network circuit inspired by famous Pavlov's dog-experiment with simulations and quantitative analyses.**

I. Introduction

THE BRAIN has excellent parallel computation capability and ultra high integration density, outperforming today's most advanced computer in the world. For this reason, building a new-type computer to emulate the brain has always been a target for scientific and engineering research [1]. However, due to von Neumann architecture's occupation in computer industries, hardware and software in modern computers are principally designed for serial computing, with separated data storage and computation units. Several decades ago, artificial neural networks, the novel computing architecture emulating the brain structure, were proposed. Neural networks are able to conduct parallel computing, and perform data storage and computation simultaneously on a single component, the synapse. To make use of these advantages, attempts have been proposed to build neural networks on silicon chips [2], [3], [4], [5]. The features of neural networks, especially the synaptic plasticity, however, are not easy to be implemented by solely utilizing CMOS transistors. Although designs of artificial synapses in analog VLSI circuits have been presented [6], the circuits are generally too complex to be integrated in large scale, diminishing the performance of the brain-like system.

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Recently, following HP Labs' demonstration of TiO_2 memristor [7] (short for *memory resistor* [8]), a plenty of researches have been focused on the device [9], [10], [11], [12]. One research direction is concentrated on its characteristic of changing internal state following current or voltage excitation. The feature is analogous to plasticity of synapses, whose weight varies according to action potentials of adjunct neurons. The device has also been proven to be suitable for neural network applications theoretically due to its high nonlinearity and dynamic property [13], [14].

Since the designs of CMOS synapses are not suitable for large scale integration due to their complexity, it is reasonable to adopt memristors into the design of artificial synapses. The combination of memristive synapses and CMOS neurons is defined as the memristive neural network, which has richer dynamic behaviors than an ordinary artificial neural network [15]. In this emerging area, pioneering works have been conducted [16], [17], [18], [19]. Some important features of neural networks, such as synaptic multiplication [20], spike-timing-dependent plasticity (STDP) [21], unsupervised learning [22], [23] etc., have been thoroughly studied and realized on memristive neural networks. Besides these features, there is another basic characteristic of neural networks, the spike-rate-dependent plasticity (SRDP), which claims the synaptic plasticity's weight is dependent on pre-synaptic spiking rate [24]. The SRDP rule is captured by the BCM model [25], and it is an extended protocol of the Hebbian learning rule [26], [27]. Li et al. realized SRDP on a single synaptic device, the Ag/conducting polymer/Ta memristor [24]. Wang et al. also implemented the protocol on a memristor, whose material is amorphous InGaZnO [28]. However, their works only considered the SRDP protocol on a single memristive device with precisely designed signals emulating action potentials. The research about the implementation of SRDP in a neural network, where advanced neural activities happen, is scarcely discussed.

In this paper, we propose a new design of memristive neural networks consisting of memristive synapses and CMOS neurons, where the SRDP protocol and some advanced neural activities are originally implemented. SPICE simulations are conducted to show bio-inspired features of these models. The neuron model capable of generating biologically realistic spikes is a modification of the leaky integrate-and-fire (I&F) model derived from Mead's work [2], [29]; the relationship between the neuron's spiking frequency and input current is established quantitatively. The synapse model is based on HP's TiO_2 memristor, in which a tunable nonlinear window function with two controlling parameters is included;

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thus arbitrary dynamics of a realistic memristor can be simulated. Integrating the neuron and synapse models, the SRDP protocol is originally implemented, underlying the mechanism of advanced neural activities including learning, associative memory and forgetting.

These neural activities are comprehensively realized on a network of three neurons and two synapses in Fig. 1. The topology of the network is an inspiration of Pavlov's classic dog-salivation experiment [30]. In the experiment, two afferent neurons' action potentials are controlled by "sign of food" and "sound of ring", respectively, and one efferent neuron's spike represents "dog's salivation". By properly setting the initial weights of synapses between these neurons, learning and forgetting activities are realized: at first, only the "food" neuron can trigger the "salivation" neuron; after simultaneous spiking of both afferent neurons, representing *learning*, the "ring" neuron is able to activate the efferent neuron solely; then, the newly built strong connection between "ring" and "salivation" neurons can be weakened by continuous stimulation of "food" neuron alone, showing *forgetting*, another significant neural activity.

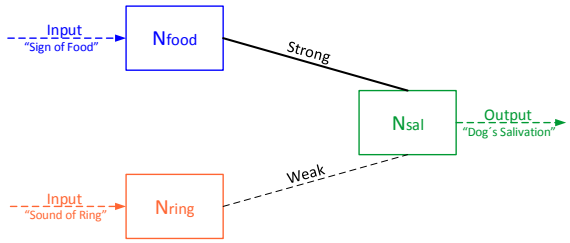

Fig. 1. The schematic of the neural network consisting of two afferent neurons N_{food}, N_{ring}, and one efferent neuron N_{sal}. Two lines connecting the afferent and efferent neurons are synapses, the solid one represents strong (or high weight) synaptic connection, while the dashed one is weak (or low weight).

Previously, several experimental demonstrations on emulating Pavlov's dog-experiment have been proposed. Pershin et al. applied micro-controllers to emulate neurons and memristor-based synapses, and Pavlov's associative memory was first implemented through softwares and codes in the controllers [31]. Another experiment was conducted by Ziegler et al., whose realization of associative memory lay in a single functional memristive device with precisely controlled signals [32]. Bichler et al. also successfully carried out the emulation on organic memristive devices, combined with a global clock signal and some micro-chips [33].

Our design in this paper provides novel perspectives inspired by, but not limited to, original Pavlov's dog-experiment. Firstly, the action potential generated by the modified leaky I&F neuron is more analogous to its biological counterpart, in respect of pulse width and spiking frequency. Secondly, the mechanism behind these neural activities is originally explained by the SRDP protocol, with visualized and clear illustration. Thirdly, we comprehensively simulate and analyse the neural activities, including not only learning and associative memory, but also forgetting, which has not been studied yet in circuit emulation of Pavlov's dog-experiment. Finally, our experiment needs neither complex auxiliary structures such as micro-controllers, nor global clock or precisely controlled signals.

The rest of the paper is organized as follows: in Section II, we present the design and analysis of the CMOS neuron model. Memristors, memristive synapses and the implementation of the SRDP protocol are discussed in Section III and IV. Then in Section V, the advanced neural activities including learning and forgetting are simulated on a neural network circuit inspired by Pavlov's experiment. Section VI concludes the paper.

II. CMOS NEURON MODEL

Among various CMOS neuron models previously demonstrated, one viable implementation is the leaky I&F model [2], [29]. The universally acknowledged MOSFET model, BSIM3v3.1 (HSPICE MOS49) [34], is adopted as the transistor in our circuit. Then the original leaky I&F neuron model is modified as in Fig. 2. Several modifications have been

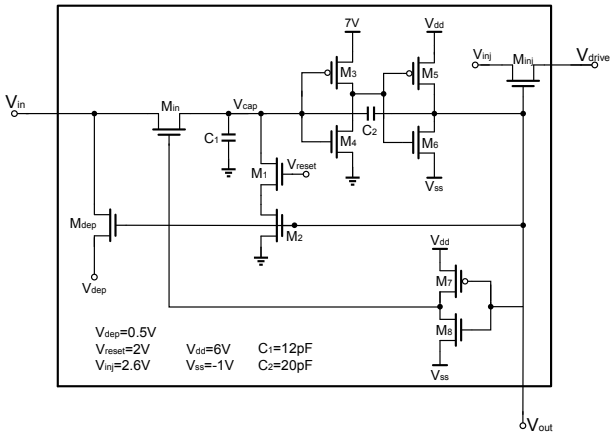

Fig. 2. The circuit of the modified $I\&F$ neuron model. MOSFETs and capacitors are utilized to construct the circuit. Some nodes are biased at certain voltages to guarantee the function. The model is regarded as a block with three terminals V_{in}, V_{out} and V_{drive}.

made to improve the electrical performance. The input port V_{in} receives signals from thousands of presynaptic neurons. If the signals are not blocked by M_{in}, they will be transferred to capacitors C_1 and C_2. As an emulation of membrane capacitors in biological neurons, C_1 and C_2 integrate input currents to increase the voltage at node V_{cap}. Once V_{cap} crosses the threshold of inverter M_3M_4, an action potential generates assisted by inverter M_5M_6 and the feedback path controlling the resistance of branch M_1M_2. During the action potential state, V_{out} is high enough to turn on transistors M_{inj}, M_{dep} and M_2, and turn off input transistor M_{in} by the means of inverter M_7M_8. Hence the injection voltage V_{inj} is directly applied to the driving port V_{drive} of the post-synapse. The on-state M_{dep} transfers V_{dep} to depress inputs, and the off-state M_{in} blocks input currents; therefore V_{cap} cannot be influenced by any inputs during the stage, representing the

refractory period in biology. Meanwhile, the low resistance branch M_1M_2 offers a leakage path for V_{cap} to discharge, thus decreasing V_{cap}. After V_{cap} falls below the threshold of inverter M_3M_4, the action potential immediately vanishes, and the neuron comes back to its original state. The electrical process of the action potential is simulated on HSPICE in Fig. 3(a), showing similarities to biological action potentials in respect of waveform, spiking width, and frequency.

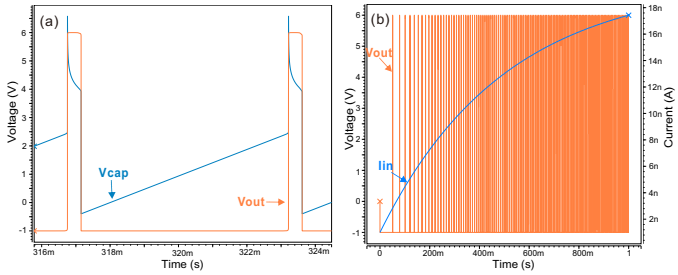

Fig. 3. Process of action potentials in the neuron model. (a) The diagram of the generation of action potentials in the neuron circuit. An action potential represented by V_{out} happens when V_{cap} exceeds the threshold voltage of the neuron. (b) The inter-spike-interval (ISI) of spikes is controlled by the injection current I_{in}. When I_{in} increases, the output spikes get intensive, and the frequency of the spikes increases accordingly.

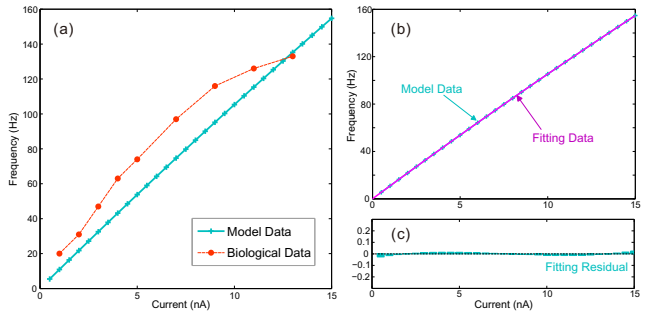

Fig. 4. Relationship between the input current I and the frequency f of spikes. (a) Comparison of $f-I$ curves between the neuron model (cross-marked) and cats' neocortex (dot-marked). (b) An equation (purple smooth line) is used to fit the $f-I$ relationship of the neuron model. (c) Residuals of the fitting in (b), showing the accuracy of the fitting.

The frequency of action potentials is determined by the value of input current I_{in} according to simulation curves in Fig. 3(b). As I_{in} increases, spikes of V_{out} get intensive, which means the inter-spike-interval (ISI) of the neuron becomes less. Then, different values of I_{in} are injected into the neuron, and the $f-I$ relationship between the spiking frequency and the input current is presented in Fig. 4(a), showing similarities in trend and slope with biological measurements of cats' neocortex [35]. Thanks to the monotonicity and smoothness of the $f-I$ curve, it is possible to quantify the relationship between f and I by a simple mathematical expression. Hence we fit the curve in Fig. 4(b) using an equation:

$$f = 10I + 1.8, \tag{1}$$

where the units of f and I are Hz and nA, respectively. The negligible residuals shown in Fig. 4(c) exhibit the relative accuracy of the fitting. With the help of Eq. (1), the spiking rate f of the neuron model can be precisely controlled by input currents I, providing a convenient approach for adjusting a neuron's firing rate, which is important for setting spiking conditions of neurons in our simulative experiments. The similarity between our model and biological neuron in respect of frequency response underlies the SRDP protocol discussed in this paper.

III. Memristors–Candidates for Synapses

Since the introduction of HP Labs' TiO_2 memristor, a growing number of models and implementations of memristors have been proposed [17], [28], [36], [37]. According to Chua's generalized concept of memristive systems [38], these memristors with various mechanisms and materials are essentially the same; every presented memristor model is able to adjust its resistance according to history, resembling the plasticity of synapses in the brain. In spite of the variance, in existing literatures, the TiO_2 memristor model is most commonly used in analysis of memristor-based systems. Therefore in this paper, we adopt the HP TiO_2 memristor model in our design and simulations.

We define $x(t)$ as the weight of the memristor,

$$x(t) = \frac{w(t)}{D} \in (0, 1), \tag{2}$$

where $w(t)$ and D are widths of doped and total regions, respectively, of the TiO_2 layer sandwiched between platinum contacts [7]. The doped region has high concentration of ions, ensuring its low resistance R_{on}, while the undoped region has high resistance R_{off} with low ions concentration. The total resistance R_{mem} of the memristor comes from the series connection of doped and undoped regions, described in the following equation:

$$R_{mem}(x(t)) = R_{on}x(t) + R_{off}(1 - x(t)). \tag{3}$$

As current passes through the device, the boundary between doped and undoped regions moves accordingly. When the applied current is conducted in positive direction, R_{mem} decreases while $x(t)$ increases, and vice-versa. If the boundary approaches terminals of the device, namely, $w(t) = 0$ or $w(t) = D$, R_{mem} is clipped to R_{off} and R_{on}, respectively, until the applied current changes its direction.

The memristor's weight $x(t)$ is considered as a state variable, and the applied current $i(t)$ and voltage $v(t)$ are regarded as input and output variables, respectively; then the model's state space representation can be:

$$\begin{cases} \dfrac{dx(t)}{dt} = ki(t)g(x(t)), \\ \\ v(t) = R_{mem}(x(t))i(t). \end{cases} \tag{4}$$

The speed of the boundary's movement, namely, the derivative of $x(t)$ in Eq. (4), is determined by the input current

$i(t)$, constant k, and window function $g(x(t))$, where

$$\begin{aligned} k &= \frac{\mu_\nu R_{on}}{D^2}, \\ g(x(t)) &= \lambda\big[1-(2x(t)-1)^{2p}\big], \end{aligned} \tag{5}$$

and μ_ν is the dopant mobility of the material. Inspired by Joglekar's window function [10], $g(x(t))$ in Eq. (5) is designed to guarantee zero speed of the boundary when it approaches terminals of the memristor. And in order to simulate arbitrary dynamics of a realistic memristor, two positive real controlling parameters, $\lambda, p \in R^+$, are added, adjusting vertical and horizontal scaling of $g(x(t))$, respectively.

Based on aforementioned descriptions, we modify the original SPICE model in [11] to be viable in HSPICE environment, and determine parameters ($R_{on} = 1M\Omega$, $R_{off} = 50M\Omega$, $D = 10nm$, $\mu_\nu = 10^{-10}cm^2s^{-1}V^{-1}$, $p = 1$, $\lambda = 1$) based on the need for emulating synapses in neural networks. Notice that the values of R_{on} and R_{off} are determined to be compatible with resistance of CMOS transistors. In spite of the numerical distinction to TiO_2-based devices [7], the order of magnitudes of these parameters can be achieved through various alternatives, such as nanoscale silicon-based memristors [17].

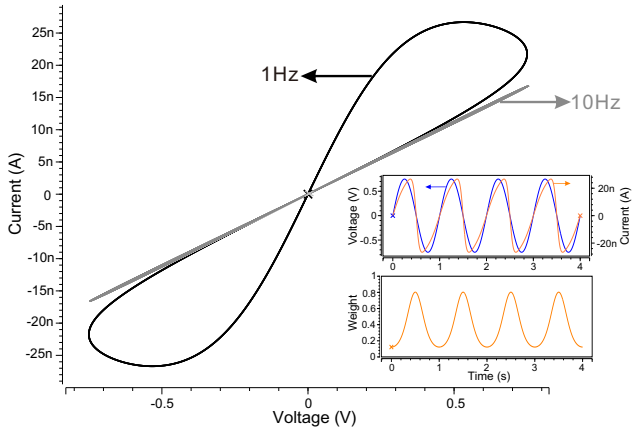

Fig. 5. The canonical $I-V$ curve of the memristor model. When a sinusoidal voltage of 1Hz is applied, the $I-V$ curve is hysteretic and zero-crossing. While the curve tends to be a straight line when the frequency increases to 10Hz. The insets show the change of the applied voltage and current (upper) and the weight (lower) of the memristor over time.

The simulation results are shown in Fig. 5, manifesting canonical properties of memristors: hysteresis, crossing original point and getting pinched when the frequency of input increases. Another important feature of the memristor model is the change of weight $x(t)$ when pulses (like spikes) are applied to its terminals. The response of $x(t)$ according to randomly generated pulse series (positive and negative) is shown in Fig. 6, where applied positive pulses increase the memristor's weight, and negative ones decrease the weight. Though biological spikes are unipolar, we use bipolar simulative spikes here to show the scalability of the memristor model. This property is key to the plasticity

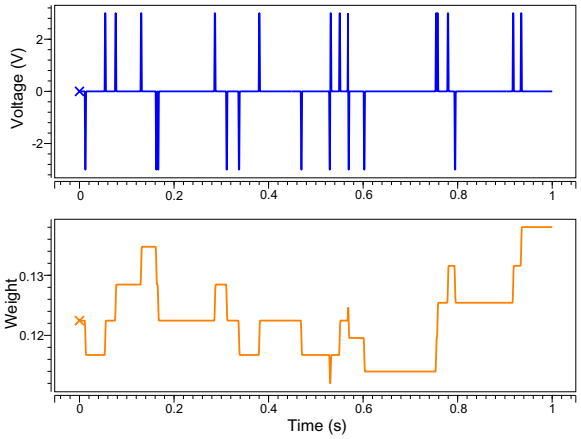

Fig. 6. The memristor's response to random generated bipolar pulses. The upper figure shows random pulses over time, and the lower one reflects the corresponding variance of the memristor's weight.

of synapses, whose weights change as well when action potentials generate.

IV. Neural Network Connection with SRDP

The key to learning and memory in the brain lies in the plasticity of synapses; hence the connection, i.e, the mimetic synapse model, is vital in the neural network design. The memristor presented above is a candidate for emulating biological synapses. However, a single memristor is not quantified for the job because of its significant change of resistance during the learning phase, which may cause the stability-plasticity dilemma in the learning system [39]. Here, we adopted a feasible synapse design described in Fig. 7 [29], where neurons are represented by blocks with three terminals, omitting the detailed circuit shown in Fig. 2. The synapse model consists of a memristor and a n-channel MOSFET, whose states are controlled by spiking patterns of N_{pre} and N_{post}. For instance, if N_{pre} is spiking while N_{post} is in quiescence, the voltage at node V_{drive} will cause the positive current injection to the memristor, increasing the weight of the synapse. But if N_{post} is spiking too, the voltage at node V_{out} of N_{post} will turn on M_s, pulling down V_{drive} to the ground, reducing the positive current injection to the memristor. It is to be noted that the practical feasibility of the integration of I&F neurons and the combination between memristors and MOSFETs has already been testified in [40] and [17].

The plasticity of synapses is symbolized by the synaptic weight $x(t)$ of the TiO_2 model. Biologically speaking, high weight means strong connection between two neurons, which results in spikes of pre-neuron (presynaptic neuron) can trigger action potentials of post-neuron (postsynaptic neuron). On the contrary, low weight or weak connection cannot guarantee the generation of these triggered spikes. The connection model is able to emulate such neural activities. Fig. 8 shows the corresponding HSPICE simulation results, where N_{pre} alone is able to activate the spiking of

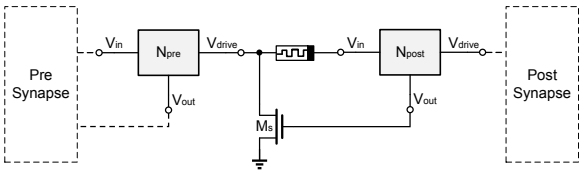

Fig. 7. The circuit of the neural network's synaptic connection. Two neuron blocks, N_{pre} and N_{post}, are connected by a synapse consisting of a memristor and a n-channel MOSFET. Action potentials of N_{pre} will cause current injection of N_{post}.

N_{post} due to the high weight (0.9) connection, but unable to trigger N_{post} with a low weight (0.1) synapse.

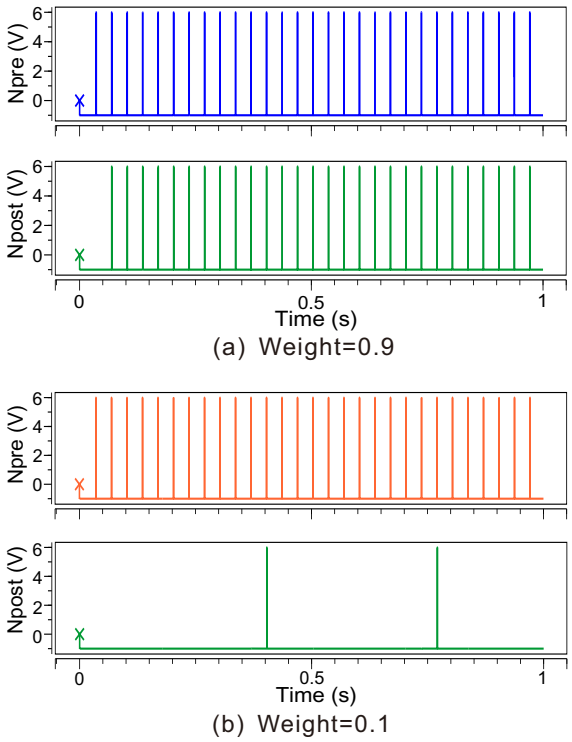

Fig. 8. Simulation results based on Fig. 7. (a) The synaptic weight is high (0.9); thus the resistance of the memrisor is low, and N_{pre} is able to activates N_{post} due to the large current injection to N_{post}. (b) The synaptic weight is low (0.1); thus the memrisor's resistance is high, and N_{pre} cannot activate N_{post} because of the little current injection to N_{post}.

The modification of synaptic weights is basis for learning and memory in neural systems. A generally accepted theory explaining this mechanism is the Hebbian learning rule [26], which expounds the adaptive synaptic plasticity following correlated excitation of pre- and post-neurons. The mathematical description of the canonical Hebbian learning rule [41] is

$$\tau_w \frac{dw}{dt} = vu, \tag{6}$$

where w is the synaptic weight, u and v represent firing rates of pre- and post-neurons, respectively. τ_w is a time constant controlling the rate at which the weight changes. The protocol discussed in this paper is SRDP, an extended protocol of the Hebbian learning rule, which varies the sign and magnitude of the change of synaptic weight according to presynaptic firing rate [27]. Specifically, a high-frequency train of presynaptic spikes results in long-term potentiation (LTP) of synapses, or the increase of synaptic weights. While a low-frequency train results in long-term-depression (LTD), decreasing synaptic weights [42]. The standard SRDP protocol form is presented in the inset of Fig. 9(a), showing weight potentiation when presynaptic input rate >10Hz, and depression for input rate <10Hz [27]. The connection model described in Fig. 7 turns out to be capable of implementing the SRDP protocol, illustrated in the main part of Fig. 9(a). That is, fixing the spiking frequency of post-neuron f_{post} at 30Hz, while changing the pre-neuron's frequency f_{pre} from 0Hz to 35Hz, the modification rate of the synaptic weight accordingly varies from about -20% (depression) to 50% (potentiation). Actually, the phenomenon of $f_{pre} = 35Hz$ and $f_{post} = 30Hz$ is a realization of the famous Hebbian rule stating, that "neurons that fire together, wire together". The frequencies are controlled by input currents, referring to the fitting Eq. (1) between $f(Hz)$ and $I(nA)$. Notice that 30Hz, the value of f_{post}, is empirically determined for properly simulating the standard SRDP protocol through analog circuits.

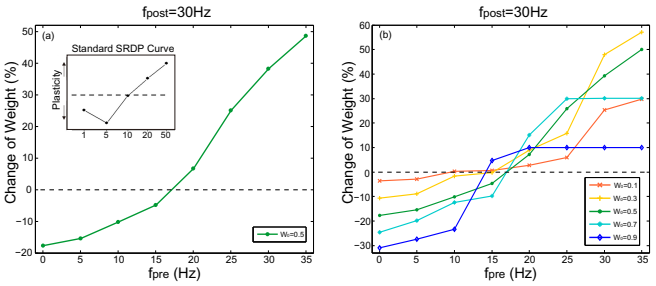

Fig. 9. The SRDP protocol is realized by appropriately controlling the input currents of N_{pre} and N_{post}. f_{post}, the spiking frequency of N_{post}, is fixed at 30Hz, while f_{pre} is the independent variable to simulate different situations for the synapse. (a) The initial synaptic weight W_0 is 0.5. When $f_{pre} < 17Hz$, the synaptic weight decreases (LTD), while the weight increases (LTP) when $f_{pre} > 17Hz$. This feature is in accordance with the SRDP protocol, whose ordinary form is presented in the inset. (b) The initial synaptic weight W_0 varies from 0.1 to 0.9. The SRDP protocol can be implemented no matter how W_0 changes.

The initial synaptic weight W_0 in Fig. 9(a) is 0.5, while experimental results reveal a dependence on W_0 of the SRDP protocol [43], demonstrating different W_0 results in different SRDP curves. Repeating the experiment with varying W_0 values, different synaptic weight changes are obtained in Fig. 9(b). However W_0 changes, the SRDP curves have characteristics in common: low f_{pre} results in LTD while high f_{pre} leads to LTP; the change of W shows greater susceptibility to the modulation of f_{pre} when W is large. Actually, this susceptibility has been discovered in biological neurons [44]. From Fig. 9 and its properties, the similarity between our model and the biological neural structure is

obvious.

V. Implementation of Advanced Neural Activities

By properly constructing a circuit consisting of the neuron and synapse models, some advanced neural activities, including learning, associative memory and forgetting, can be achieved. In order to show these activities, a network inspired by Pavlov's famous dog-salivation experiment is built as in Fig. 10. The network consists of two afferent neurons N_{food}, N_{ring} and one efferent neuron N_{sal} (see Fig. 1). N_{food} generates spikes when "sign of food" signal transfers in, and N_{ring} excites when "sound of ring" signal comes. These two neurons are both connected to N_{sal} with synapses. The synaptic weights, however, are different. According to Pavlov's original experiment, the spikes generated by N_{food} can trigger N_{sal} to activate, representing "salivation". The activation of N_{ring}, however, is not able to trigger N_{sal}. For this reason, a high weight (0.9) is set to the synapse between N_{food} and N_{sal}, while a low weight (0.1) is set to the one between N_{ring} and N_{sal}. These weight configurations guarantee the initial condition of the experiment. Then, different currents are injected to afferent neurons to construct various spiking conditions during the simulation.

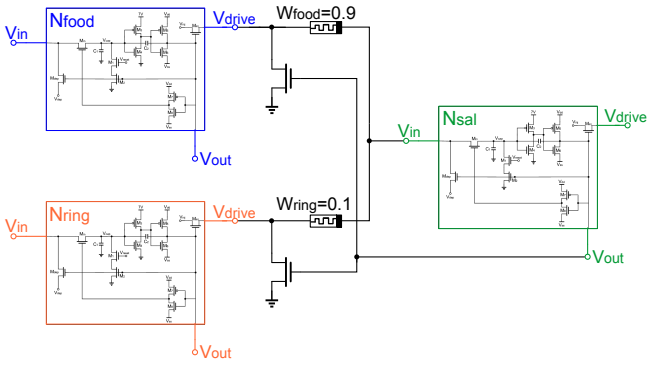

Fig. 10. The circuit of a neural network inspired by Pavlov's canonical experiment on dog's salivation. Two afferent neurons, N_{food} for "sign of food" and N_{ring} for "sound of ring", are connected to an efferent neuron N_{sal} representing "dog's salivation" by two synapses. The initial weights are 0.9 and 0.1 for W_{food} and W_{ring}, respectively, guaranteeing the initial strong connection for "sign of food" and weak connection for "sound of ring".

Detailed simulation procedures and results are presented in Fig. 11. We divide the whole process into five stages - S_1 to S_5. In stage S_1, N_{food} and N_{ring} both activates alone for a period of time; it is not surprise to see the responding spikes and quiescence of N_{sal}, to N_{food} and N_{ring}, respectively. And the changes of W_{food} (synaptic weight between N_{food} and N_{sal}) and W_{ring} (synaptic weight between N_{ring} and N_{sal}) are negligible. In stage S_2, the *learning* stage, N_{food} and N_{ring} fire together causing N_{sal} to activate, mainly owing to N_{food}. Notice the weights' change during the stage, i.e., while W_{food} reaches and retains at upper bound (1.0), W_{ring} increases abruptly, realizing the *learning* function of the network. Therefore at the beginning

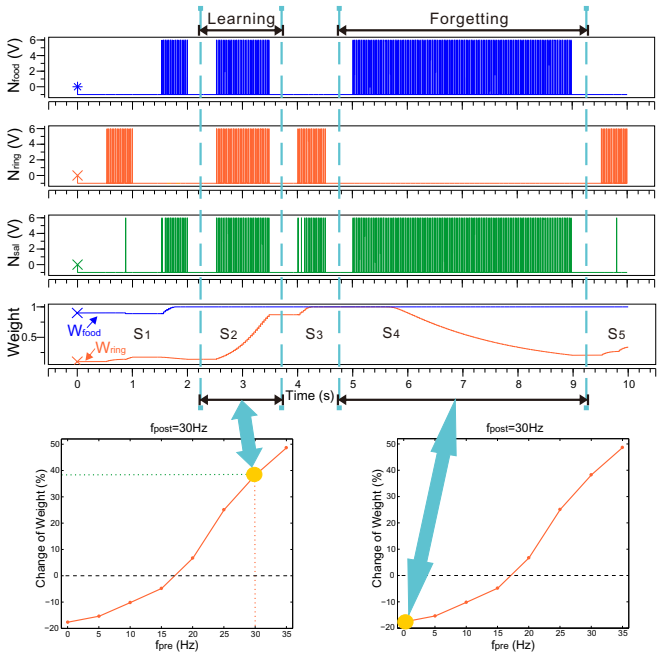

Fig. 11. Simulation results of the circuit in Fig. 10 combined with explanation by the SRDP protocol. Three output voltage over time plots on top show spiking and quiescence of N_{food}, N_{ring} and N_{sal}, respectively. All spiking states of these neurons are controlled to be fixed at around 30Hz. Below the plots, the evolvement of synaptic weights W_{food} and W_{ring} over time is presented. At the bottom, two SRDP curves dot-marked with the synaptic situation (specific values of f_{pre} and f_{post} for *learning* and *forgetting* stages) are shown. The whole process is divided into five stages S_1 to S_5 for clear analysis.

of stage S_3, W_{ring} has jumped to a relative high weight (0.85). This high weight makes it possible for spikes of N_{ring} activating N_{sal} solely; i.e., the "sound of ring" alone can cause "dog-salivation" during stage S_3. The phenomenon shows the ability of *associative memory* after *learning* of the network. Stage S_4, the *forgetting* stage, is a long period of time, during which N_{food} undergoes a frequent excitement, while N_{ring} stays quiescent all the way. The corresponding weights also undergo a meaningful procedure: while W_{food} still retains at upper bound, W_{ring}, however, experiences a relatively smooth but obvious decrease, so at the end of the stage, W_{ring} comes back to a low weight (0.2). This stage emulates *forgetting* activity successfully: that is, the newly established strong synaptic connection in the brain will gradually weaken if there is no repetitive activation of the synapse while other synapses manifest excitement frequently. Hence after the *forgetting* procedure, in stage S_5, when N_{ring} fires alone, it is not surprise to see the non-response of N_{sal}.

The principle behind the simulation results, especially the *learning* and *forgetting* activities, can be explained by the SRDP protocol represented at the bottom of Fig. 11. In the *learning* stage S_2, N_{ring} alone is not able to trigger N_{sal} at the beginning, but the simultaneously firing of N_{food} causes spikes of N_{sal}, thus creating a condition of $f_{pre} = 30Hz, f_{post} = 30Hz$ for synapse W_{ring}. The condition results in the synaptic weight potentiation of about 40%

according to the SRDP protocol and leads to the increase of weight during the *learning* stage. Similarly, during the *forgetting* stage S_4, N_{ring} stays quiescent all the time, while N_{food} undergoes a lasting activation and leads to action potentials of N_{sal}. A condition of $f_{pre} = 0Hz, f_{post} = 30Hz$ for synapse W_{ring}, therefore, is established. Then, based on the SRDP protocol, the synapse becomes depressed at a rate of about -18%: the decreasing of weight comes into being. Actually, the *forgetting* activity of W_{ring}, resulted from the influence of N_{food}'s lasting activation, is in accordance with the biological phenomena, where some kinds of synapses undergo LTD because of inputs of nearby or lateral synaptic terminals [45], [46].

VI. Conclusion

The aforementioned sections demonstrate the feasibility of our neuron and memristive synapse models to emulate neural properties, such as biologically realistic spikes, current-controlled action potentials and adaptive synaptic plasticity etc. Owing to the memristive synapse, the neural network consisting of these models originally shows the capacity of realizing the SRDP protocol. Moreover, advanced neural activities including learning, associative memory and forgetting are comprehensively implemented using the network configured in Fig. 1, inspired by canonical Pavlov's dog-experiment. Thanks to the nanoscale of memristors, high integration density friendly large scale memristive neural network circuits can be built following the principle discussed in this paper, accelerating the generation of new-type brain-like learning system, and contributing to a variety of applications such as pattern recognition, machine learning, and nonlinear adaptive control problems.

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