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# Analog Memristive Time Dependent Learning Using Discrete Nanoscale RRAM Devices

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***Abstract*—We propose a scheme that mimics the analog time dependent learning characteristics of biological synapses using a small set of discrete nanoscale RRAM devices whose switching voltages vary stochastically. Using numerical models and simulations, we demonstrate that a voltage limited analog memristor operating in the tunneling regime and a parallel combination of $< 10$ RRAM devices having discrete resistance states (two resistance states – high and low), can both be employed as artificial synapses with similar statistical performance. We also show that by appropriately choosing the programming voltages and hence the switching probability of the RRAM devices, it is possible to tune the relative conductance of the synaptic element anywhere in the range of $2 - 100$. This paper thus shows the possibility of using discrete RRAM devices to realize an analog functionality in artificial learning systems.**

***Keywords*—Spike Timing Dependent Plasticity, Memristor, Neuromorphic Computing.***

## I. Introduction

Reverse engineering the operating principles of the human brain and building computational hardware mimicking its key algorithmic features is a grand challenge of this century [1]. Thanks to focused research to establish the underlying principles of computation employed by biological systems, it is now becoming clear that information is encoded, transmitted and processed in the time of arrival of spikes at the neurons, which are the computational nodes in the brain. The pathways of information processing are determined by the effective strength of the connections between the neurons – the synapses. It is now well established that the state of the synapse is determined primarily by the time of arrival of spikes at the pre- and post-synaptic neurons. Spike Timing Dependent Plasticity (STDP) has emerged as the fundamental mechanism underlying cognition, learning and memory [2] (Figure 1).

Recent advances in nanotechnology has buoyed the hopes of building area and power efficient hardware mimicking the operating principles of the brain [3]. One of the most promising developments in the area of nanoelectronic devices in the past decade has been the demonstration of the memristor [4]. Memristors are passive two terminal devices with variable resistances that depend on the history of current flow through them [5]. Nanoscale memristive devices offer a wide range of advantages such as device

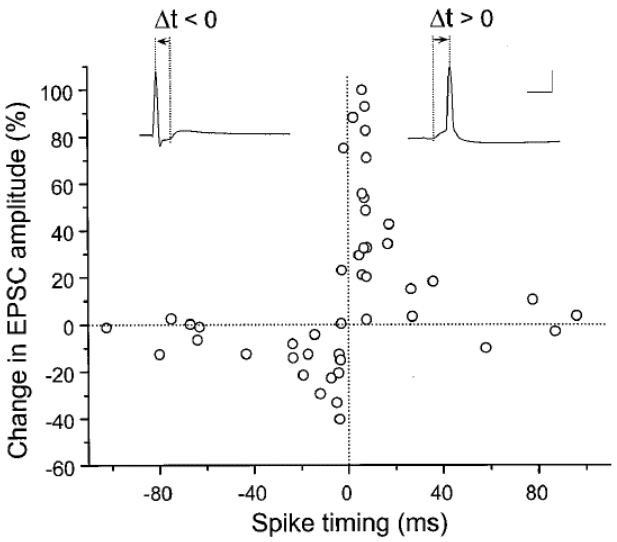


Fig. 1. Change in synaptic-efficacy due to spiking of two consecutive neurons connected through a synapse in biological systems. Experimental data taken from [2] demonstrating the classic Spike Timing Dependent Plasticity (STDP) rule for biological synapses.

scalability, compatibility with CMOS technology, low power consumption and reasonable switching speed. Since the recent demonstration of a nanoscale ion-drift based device that showed memristive properties [4], memristors have attracted immense attention also in the field of neuromorphic engineering, where, one of the main challenge is to mimic synaptic plasticity in power and area efficient hardware devices. In artificial learning systems, memristive devices have been envisioned as *artificial synapses* that mimic synaptic plasticity, typically demonstrated by establishing that it will exhibit STDP or other timing dependent adaptation rules. The STDP behavior across any two terminal device is demonstrated when it exhibits an expected set of trends in the conductivity modulation as a function of the temporal separation between two voltage pulses applied at the two terminals. The voltage pulses could be shaped in the form of the action potential waveform [3], [6], though other ideas using more complicated waveforms or complex signaling schemes that require precise clocking have been proposed earlier [7].

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While the synapse and its associated learning behavior is believed to be an analog paradigm, it is the primary objective of this work to demonstrate that digital devices may also be tailored for a similar synaptic functionality. Using numerical simulations, we first show that the STDP behavior may be captured by a nanoscale ion-drift memristive device in the tunneling regime [4]. Use of memristors in artificial neuromorphic domain to achieve synaptic plasticity has already been shown in [8], [9], [10], [11]. While most of the fabricated memristive devices show an on-off conductance ratio greater than 100 [4], we particularly tune or choose our pre-synaptic and post-synaptic programming pulses to partially switch our analog device so that the modified on-off ratio is within a range of approximately 2, on par with biological systems [2]. We then propose a scheme to mimic this analog memristive time dependent learning, using a small set (9 or 16) of discrete nanoscale RRAM devices whose switching voltages vary stochastically [12]. The two schemes, i.e., the analog memristive switching and the discrete switching schemes are then shown to be of similar statistical performance.

This paper is organized as follows. In the following section, we describe the simulation set up. Section III and IV will focus on how the essential STDP feature is captured by the analog memristive switching, which we term as *memristive switching* and the digital scheme, which we term as the *discrete switching* scheme respectively. Section V will demonstrate the statistical aspects of the two paradigms and establish the similarity between them.

## II. Simulation set up

The biological nervous system consists of a network of neurons that are connected to each other through an intricate mesh of plastic synapses. Each neuron receives input stimuli/signals from thousands of pre-synaptic neurons and transmits signals to thousands of post-synaptic neurons. When a group of input/pre-synaptic neurons fire within a small time window, the cumulative depolarization of the output neuron exceeds a threshold voltage, resulting in an 'all-or-none' action potential. For the purpose of evaluating methods for implementing plasticity, we simulate a network of $n$ input neurons stimulating one output neuron. We denote this architecture as the $n \times 1$ network. Typically, $n$ has to be a large number (typically $> 100$) to account for the fact that an output neuron has to be depolarized by several input neurons before it can generate an action potential. In our simulations, $n$ is chosen to be 100. A schematic of our simulation network for both the memristive and the discrete scheme is depicted in Figure 2.

The dynamics of the output neuron is modeled using the *leaky integrate and fire model*, given by the equation:

$$C\frac{dV}{dt} = -g(V - E) + \sum I_{syn} + \sum I_{ext}, \qquad (1)$$

where $g$ is the leakage conductance, $E$ is the resting potential of the neuron and $I_{syn}$ is the current flowing into the neuron from the pre-synaptic neurons, based on the potential of the input neuron and the strength of the synaptic connection. $I_{ext}$ represents the current flowing into the neuron due to external input stimulus. An appropriate stimulus at the input neuron causes it to spike, which in turn generates

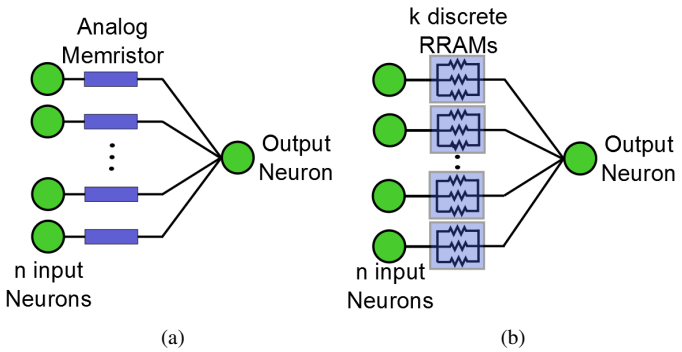



Fig. 2. Schematic of the simulated network for (a) analog memristor (b) $k$ discrete RRAM devices connected in parallel to form the synapse. In our simulations, we study the dynamics of the network for $n = 100$ and $k = 4, 9, 16$.

the synaptic current. The sum of the currents from all input neurons is integrated at the output neuron, thereby depolarizing the output neuron. The output neuron will spike when its membrane potential reaches a certain threshold value. In biological neurons, the neuron resting potential hovers around $-70\,\text{mV}$ and the firing threshold hovers around $-40\,\text{mV}$. In our simulation, the resting potential is taken to be $0\,\text{mV}$.

In order to implement timing dependent learning in our artificial synaptic devices, we have chosen the scheme presented in [3]. According to this scheme, every neuron, upon spiking, sends a pre-synaptic waveform towards the axonal end, and a post-synaptic waveform towards its dendritic end. We illustrate this in Figure 3 which shows a neuron $n_s$, receiving inputs from $n_i$ neurons and connecting to $n_o$ downstream neurons.

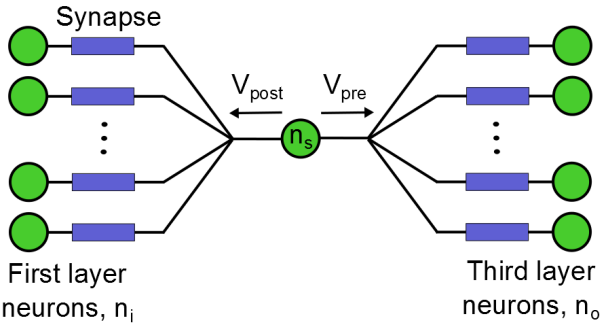



Fig. 3. Schematic of the adopted programming methodology [3]. Each neuron upon spiking sends a pre-synaptic programming waveform on all its axonal terminals and a post-synaptic programming waveform on all its dendritic terminals.

Our main objective is to show that Spike Timing Dependent Plasticity behavior of synapses can be achieved by using either (i) an analog memristor or (ii) a parallel combination of discrete RRAM devices. The classic Spike Timing Dependent Plasticity (STDP) rule states that a synaptic connection is potentiated or strengthened when a pre-synaptic neuron firing occurs a few milliseconds before a post-synaptic firing and depressed or weakened when a post-synaptic firing occurs a few milliseconds before a pre-synaptic firing [2], [13] as shown in Figure 1.

One of the key motivations for building hardware circuits mimicking neural networks is the possibility to accelerate the dynamics and implement learning and decision making in time scales faster than that is possible in normal biological systems or software simulations. We have chosen to study the dynamics for an acceleration factor of $50$. However, our scheme is flexible and can be used to achieve desired acceleration factors over a wide range by adjusting the parameters of the programming waveforms used to control the state of the artificial synapse. In biological systems, a causal pair or an anti-causal pair can cause synaptic strengthening or weakening when the delay between the pre-synaptic and post-synaptic action potential is at most $\pm 80\,\text{ms}$ (approx). An acceleration factor of $50$ implies that synaptic changes in our system will occur for a delay of at most $80\,\text{ms}/50 = 1.6\,\text{ms}$ between the pre-synaptic and post-synaptic action potentials.

In biological systems, the firing of neurons are highly irregular and stochastic. In our simulation, this is modeled by a Poisson arrival process. The input neurons are stimulated with independent Poisson stimuli with a mean arrival rate of $1800\,\text{s}^{-1}$. This stimulation rate is enough to cause firing of the output neuron as well as to cover the entire range of pre-synaptic to post-synaptic firing delay between $0$ and $\pm 1.6\,\text{ms}$.

In artificial neuromorphic systems, the characteristics of the synapse are to be mimicked by an equivalent two terminal device. Our analysis is based on the timing dependent plasticity scheme proposed in [3]. As per this model, a spike will create a pre-synaptic or post-synaptic programming waveform of the form

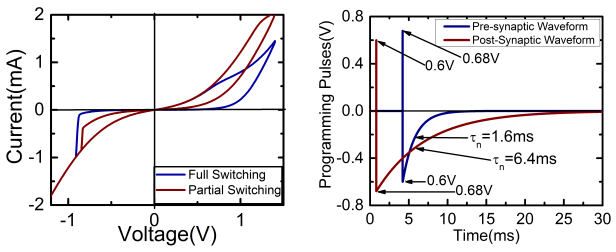
$$\begin{aligned} V = V_{Max}^{+} e^{-t/\tau_p}(u(t) - u(t - T_w)) \\ - V_{Max}^{-} e^{-(t-T_w)/\tau_n} u(t - T_w) \end{aligned} \tag{2}$$

The initial part has a peak amplitude $V_{Max}^{+}$ with decay constant $\tau_p$ and pulse width $T_w$. This part is followed by a negative exponential pulse that has a peak amplitude of $V_{Max}^{-}$ with a decay constant $\tau_n$. Typically $\tau_n \geq 20\tau_p$. An overlapping set of pre-synaptic and post-synaptic pulses can cause an increase in the magnitude of the voltage drop across the electrical synapse, and depending on the sign, cause synaptic strengthening or weakening. Implementation of this type of exponential programming pulses has already been discussed in [3]. In our simulation, around $40\%$ of the input neurons having strong synapses are able to elicit a spike in the output neuron provided they fire together within a time interval of $400\,\mu\text{s}$. However this number can vary depending on the timing interval itself. A refractory period of $10\,\mu\text{s}$ is implemented for each neuron in our simulation.

## III. STDP WITH ANALOG MEMRISTIVE DEVICES

Memristors are nanoscale devices having ideally a set of stable resistance states. An analog memristor is characterized by continuous set of resistance states in between its two extremum states. Memristors are hence characterized by a pinched current-voltage hysteresis loop [5] and a non-volatility in the resistance when no currents pass through the device [5]. On the application of appropriate electric field, the state of the device may change from a high resistance state to a low resistance state. This process is called the SET operation. Application of an electric field in the opposite direction results in the resistance of the device to change from a low resistance state to a high resistance state. This process is called the RESET operation. Development of well-controlled, analog memristive devices as well as their characterization and physical modelling remains an active area of research at this point as the field is in its infancy [14]. The fabrication procedure as well as the materials used to form the electrode metals and the dielectric determines the switching properties of the device. Implementation of a synapse with a single memristive device calls for a device with non-linear current-voltage characteristics. Control over the switching phenomenon of the device is another requirement, so that all the resistance states of the device between the extremum states are accessible.

For our simulations, we need a model for the memristor that captures the essential device physics and matches relevant experimental data. Although various models are available in literature, most of them fail to completely explain the observed characteristics. One of the earliest works to capture the essential features of memristive switching was proposed in [15], but it does not do justice to the device physics in detail. Also, it can be shown that with our proposed scheme, devices modeled using the simple models developed there [15] cannot reproduce the STDP characteristics without incorporating a rectifying device in series with it. Hence, we chose the physics based model proposed by Pickett et al [6] for our analysis. This model explains the dynamical $I - V$ characteristics of a $\text{Ti}/\text{TiO}_2$ based memristive nanodevice with the help of the Simmons tunnel barrier model [16]. Simmons tunnel barrier model explains the phenomenon of tunneling of electrons through an energy barrier (insulating film) when a suitable electric field is applied across it. The memristive nanodevice modeled in [6] consists of a $215 \pm 6\,\Omega$ linear resistor in series with a thin insulating film. The current through this insulating film is solely governed by Simmons tunnel barrier model. On application of suitable electric field through the device, the mobile dopants will either spread or accumulate (depending on the direction of application of electric field) thereby varying the width of the insulating film and exhibiting memristive behavior. As described in [6], the device is characterized by fast SET operation and a gradual RESET operation.




(a) (b)

Fig. 4. (a) Simulated partial and complete switching characteristics of a memristor using the Pickett's Model [6]. A triangular voltage sweep with amplitude of $1.4\,\text{V}$ and time period of $20\,\mu\text{s}$ (blue curve) and $100\,\text{ms}$ (red curve) was applied to the memristor. (b) An exemplary pre-synaptic and post-synaptic programming waveforms applied to the analog memristor.

In biological systems, it is observed that the synaptic efficacy of a strong synapse is typically two to four times

larger than that of a weak synapse. However, most fabricated memory switching devices have an on-off conductance ratio greater than 100. This poses a problem in mimicking biological neural networks as a synapse replaced by a memristor would depolarize the output neuron 100 times more in the high conductance state than in the low conductance state. The problem can be alleviated by suitable design architecture (for example, adding a logarithmic amplifier can reduce the depolarization of the output neuron). However, a simpler solution is to tune the amplitude of the pre-synaptic and post-synaptic waveforms such that the memristor doesn't switch completely to it's extremum states, that is, the memristor changes back and forth within a fraction of it's total conductance range. Power minimization calls for the use of the low conductance range of the device. However, the SET process cannot be controlled by voltage. The trick is to control the RESET process so that the device does not switch off completely to it's off-state. Hence, we have chosen to utilize the high conductance range of the device. The amplitude of pre-synaptic and post-synaptic waveforms are chosen so that the conductance varies approximately between the maximum conductance state $G_{Max}$ and $G_{Max}/2$.

Since Pickett's model is inherently non-linear with a voltage dependent conductivity, we have chosen to report the effective resistance of the artificial synapse by measuring the current through the device, when $0.5\,\mathrm{V}$ is applied across it. Figure 4(a) shows the simulated I-V characteristics of the memristor when it is allowed to switch partially. The pre-synaptic and post-synaptic programming waveforms based on 2 are shown in Figure 4(b). The parameters for pre-synaptic programming waveform are $V^{+}_{Max} = 0.68\,\mathrm{V}$, $V^{-}_{Max} = 0.6\,\mathrm{V}$ and $\tau_n = 1.6\,\mathrm{ms}$. For post-synaptic programming waveform, the parameters are $V^{+}_{Max} = 0.6\,\mathrm{V}$, $V^{-}_{Max} = 0.68\,\mathrm{V}$ and $\tau_n = 6.4\,\mathrm{ms}$. The value of $\tau_p$ for both pre-synaptic and post-synaptic programming waveforms is $2\,\mu\mathrm{s}$ and $T_w = 10\,\mu s$.

During the overlap between the pre-synaptic and the post-synaptic waveform, maximum voltage will drop (and hence maximum current will flow) through the synapse when the positive peak of post-synaptic waveform will coincide with the negative peak of the pre-synaptic waveform for a small positive value of $\Delta t$. Hence maximum change in synaptic strength will occur. With increasing values of $\Delta t$, the maximum voltage (and hence current) across the synapse at the instant of overlap will decrease exponentially. Hence the relative change in synaptic strength will also decrease with increasing $\Delta t$. Similar phenomenon occurs for negative values of $\Delta t$.

The STDP points of the analog memristive synapse following Pickett's model at the end of application of 2000 pulse pairs are shown in Figure 5(a). Note that we are able to reproduce the biological STDP curves to a high degree of accuracy. However, due to device limitations (SET process being fast and current-controlled), all the resulting STDP points do not lie completely within the exponential envelop.

## IV. STDP WITH BINARY STOCHASTIC DEVICES

We now develop a scheme that enables nanoscale Resistive Random Access Memory (RRAM) devices with stochastic switching properties to be used for implementing

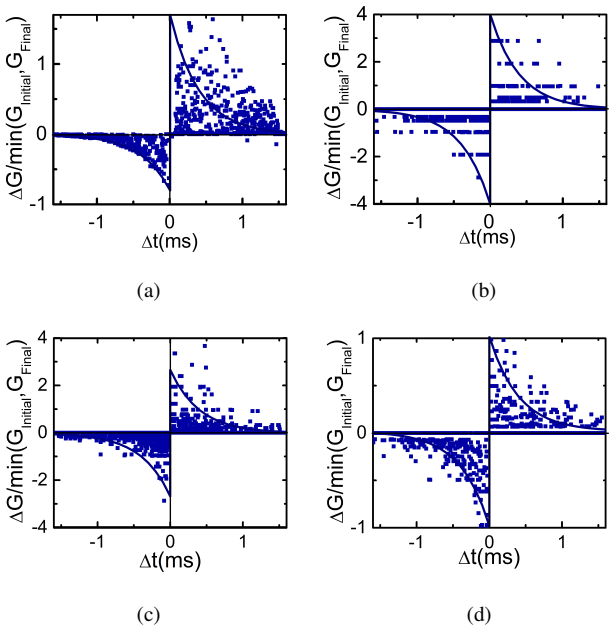
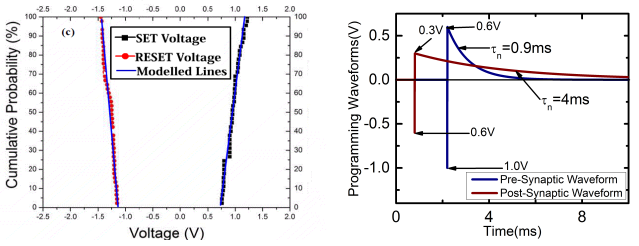



Fig. 5. STDP with (a) synapse consisting of an analog memristor along with an eye-guide exponential fit. (b), (c) and (d) are equivalent STDP simulation results for synapse with 4, 9 and 16 RRAM devices respectively. The reproduced simulation curves can match the exponential form of biological STDP curves to a high degree of accuracy.

STDP in neuromorphic learning systems. RRAM is a two terminal switching device essentially having two resistance levels. However, recent research has also shown that RRAM devices can be programmed to multiple stable intermediate resistance states by controlling the applied programming voltages/currents [17], [18], [12], [19]. In our simulation, we assume RRAM devices with essentially two resistance states – high resistance state and low resistance state. Neuromorphic applications employing stochastic learning with binary synapses has been discussed in [20], [21], [22].

In most of the fast switching RRAM devices, the switching voltage varies stochastically within a certain range. Stochastic variations of switching voltages have been discussed in detail in [23], [24], [25]. It has been observed that the probability of switching increases almost linearly with the applied voltage. Figure 6 shows the variation of switching probability with increase in voltage magnitude of a fabricated RRAM device.

We will now show that this stochastic variation in switching voltage may be used to mimic the analog STDP behavior of biological synapses. Figure 6 shows the pre-synaptic and post-synaptic voltage waveforms used in our simulations. The parameters for pre-synaptic programming waveform (described by equation 2) are $V^{+}_{Max} = -1\,\mathrm{V}$, $V^{-}_{Max} = -0.6\,\mathrm{V}$ and $\tau_n = 0.9\,\mathrm{ms}$. For the post-synaptic programming waveform, the chosen parameters of equation 2 are $V^{+}_{Max} = -0.60\,\mathrm{V}$ , $V^{-}_{Max} = -0.30\,\mathrm{V}$ and $\tau_n = 4\,\mathrm{ms}$. We have chosen the value of $\tau_p$ for both pre-synaptic and post-synaptic action potential to be $1\,\mu\mathrm{s}$, assuming that the device can switch in less than $100\,\mathrm{ns}$. We have simulated the $100 \times 1$ neural network with the synapses consisting of $k$ parallel RRAM devices. We have chosen $k$ to be a perfect square integer, because of ease of fabrication of such



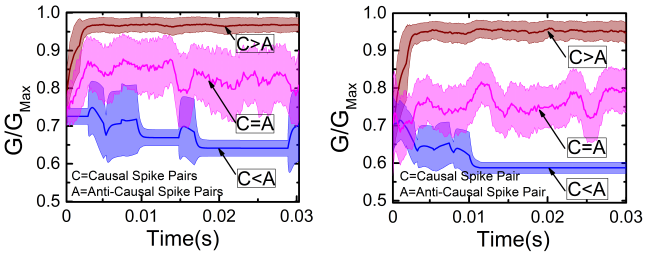

(a) (b)

Fig. 6. (a) Variation of the switching probability of the discrete RRAM device with voltage (experimental data taken from [25]). In our simulations, the probability of switching is assumed to increase linearly with the potential drop across the device. The blue lines show the modeled data used for simulation. (b) The pre-synaptic and the post-synaptic programming waveforms used in simulation are based on the probability trends in (a).

arrays in crossbars. We have simulated the $100 \times 1$ neural network with synapses consisting of $k$=4, 9 and 16 RRAM devices in parallel. A synapse consisting of "$k$" parallel RRAM devices would have $(k+1)$ resistance levels and at most $k(k+1)/2$ STDP levels. On application of the programming voltage, the individual RRAMs in the synapse will switch probabilistically, but by using larger number of discrete devices in parallel, we expect to get a continuous change in the STDP graph. Our goal is to determine how small an array of discrete devices is necessary to closely mimic the analog STDP curve shown in Figure 5(a).

In our simulation, the experimental data from [25] is used. These devices have high resistance states around $100\,\mathrm{K}\Omega$ and low resistance state around $1\,\mathrm{K}\Omega$ [25]. As stated earlier, the on-off conductance ratio greater than 100 poses problem in designing artificial neural networks. One way this problem can be alleviated is by using a suitable resistor of appropriate magnitude in parallel to the synapse so that the effective on-off resistance becomes almost 2. For example, a $0.25\,\mathrm{K}\Omega$ resistance in parallel with the synapse consisting of 4 RRAMs gives an effective on-off ratio of approximately 2. However this will cost fabrication density and unnecessary power dissipation. A more efficient solution is to keep at least one of the RRAMs in ON state all the time by reducing the RESET probability of the devices. This can be done by choosing lower amplitudes for the pre-synaptic and post-synaptic waveforms so that the probability of RESET never reaches 1. In our simulation, the maximum RESET probability is set to 0.4 by limiting the maximum negative voltage drop across the device to $-1.3\,\mathrm{V}$. This is based on the assumption that that the probability of RESET switching increases linearly from 0 to 1 when the voltage decreases from $-1.2\,\mathrm{V}$ to $-1.45\,\mathrm{V}$ respectively.

Figures 5(b), (c) and (d) show the simulated STDP graphs for synapses made of 4, 9 and 16 RRAM devices with stochastic switching characteristics. It can be seen that the discrete levels are clearly visible when the synapse is made of 4 parallel RRAM devices. However, the curve becomes more continuous when the number of parallel RRAM devices within a synapse is increased. A synapse made of 9 RRAM devices shows a good continuity in the STDP graph. So, we state that for the chosen RRAM devices, we can get an almost continuous STDP graph with a synapse consisting of at least 9 parallel RRAM devices. The continuity of the STDP graph could be improved by increasing the number of parallel RRAM devices in a synapse. However, that results in higher power and area consumption. So, a tradeoff has to be made depending on the precision required. We have hence shown that digital/discrete RRAM devices with stochastic switching behavior may also be tailored to give Spike Timing Dependent Plasticity.




(a) (b)

Fig. 7. Temporal evolution of conductivity in a group of synapses comprising of (a) one analog memristive device, and (b) parallel combination of 9 RRAM devices. The average of the group of synapses is shown for three different cases - more anti-causal spike pairs than causal spike pairs (solid blue line), almost equal number of causal and anti-causal spike pairs (solid pink line), more causal pairs than anti-causal pairs (solid brown line). The shaded region depict the standard deviation in each case. Similar time dependent variations are seen for the analog memristive device and the parallel combination of 9 RRAM devices.

### A. *Capturing STDP in a group of synapses*

When the pre- and post-synaptic neurons of a synapse repeatedly spike in causal order, the average synaptic strength is expected to see an overall increase in conductivity. The conductivity should decrease, if on the other hand, the temporal order of the spiking is reversed. This must in general be true for a group of synapses as well, if they all experience similar number of causal or anti-causal spike pairs. Both the schemes given in this paper capture this ensemble average property of STDP. In our simulation, the group of 100 input neurons were excited with stimuli at the rate of $1800\,\mathrm{s}^{-1}$ and $2600\,\mathrm{s}^{-1}$ respectively. Since we use the leaky integrate and fire model to stimulate the output neuron in our simulations, the spiking rate of the output neuron does not increase linearly with the spiking rate of the input neurons. It was observed than when the input neurons were spiking at an average rate of $1800\,\mathrm{s}^{-1}$, the output neurons spiked at a lower rate compared to the input neurons. This means that on average, synapses will see more anti-causal spike pairs than causal ones. So, the average strength of the group of synapses must decrease. This is clearly seen in Figure 7 (solid blue lines) for both analog memristive switching devices and parallel combination of discrete RRAM devices.

When the input neurons were spiking at a rate of $2600\,\mathrm{s}^{-1}$, the output neuron spiked at almost the same rate as the input neurons. So, synapses on average would see equal number of causal and anti-causal pair of spikes and the average synaptic strength of the group of synapses should more or less remain constant (solid magenta lines in Figure 7).

To study the dynamics of the group of synapses when they encounter more causal spike pairs then anti-causal ones, we chose 80 random input neurons to spike at an average rate of $2600\,\mathrm{s}^{-1}$ and the remaining 20 neurons were provided a large current so that they spike at a larger rate of $26000\,\mathrm{s}^{-1}$. Due to higher stimulation rate of these 20 input neurons, the spike rate of the output neuron will also increase. So, on an average 80 synapses will see more causal spike pairs than anti-causal spike pairs. So, the average synaptic strength of the group of 80 synapses will see an overall increase as shown by the solid brown lines in Figure 7.

## V. Statistical Comparison between Memristive and Discrete Switching Schemes

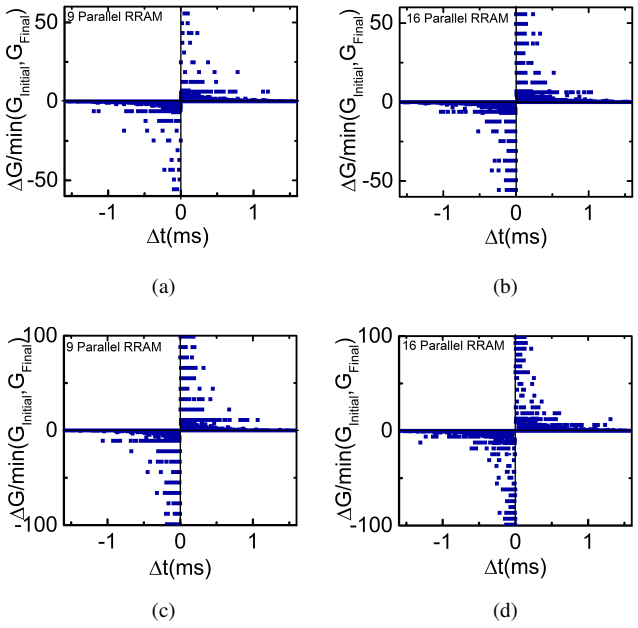



Fig. 8. The maximum value of average conductance change seen by a synapse made of 9 (left) and 16 (right) parallel RRAM devices with maximum RESET probability set to 0.7 (top) and 1 (bottom). Maximum on-off synaptic conductance ratio up to 100 can easily be achieved by adjusting the maximum RESET probability of the RRAM devices. By controlling the amplitudes of the pre-synaptic and post-synaptic programming waveforms, we can also tune this ratio up to 100.

Both the schemes described above can be used to implement synapses in a neural network. The advantage of these schemes is that the effective resistance ratio of the synapses can be controlled by tuning the maximum voltage drop across the synapse. So far, we have chosen the parameters of the programming waveform to demonstrate relative conductivity change by a factor of 2, but by appropriately tuning these parameters, we can easily achieve other desired on-off conductance ratios up to a factor of 100, as shown in Figure 8. Another advantage of these schemes is that this implementation is devoid of CMOS and rectifying devices, eliminating the need for buffering and matching circuits. Mismatches in device switching voltage and impedance will not affect the performance of the system as long as they remain in a tolerable range. Since the sum of all synaptic currents is integrated at the output neuron, small mismatches in device impedance will not influence the performance of the hardware.

Depending on the area of application, either the analog memristor or binary switching RRAMs may be preferable for synapse implementation. The advantage of an analog memristor is that implementation of a synapse consists of one single nano-scale device. The advantage of binary-switching RRAM devices, on the other hand, is ease of fabrication. Parallel combination of RRAMs in synapse consume more area and power. It has been stated in [3] that an artificial synapse consisting of a series combination of a diode and a RRAM consume at least 10 times less area and power compared to digital synapse implementation with CMOS circuitry. So, a combination of 9 parallel RRAM devices for a synapse will reduce the area by at least a factor of 2 compared to digital implementation of synapse with CMOS circuitry (assuming that the cell size of each fabricated device is $4F^2$, where $F$ denotes the minimum *feature size*). In this section, we will show that both these schemes have almost identical statistical properties.

To study the statistical property of both schemes, a train of Poisson stimulus of average arrival rate of $2600\,\mathrm{s}^{-1}$ were applied to the input neurons. This rate was chosen as a reference because at this rate of input stimulus, the average spiking rate of the output neuron is almost equal to the average spiking rate of the input neurons.

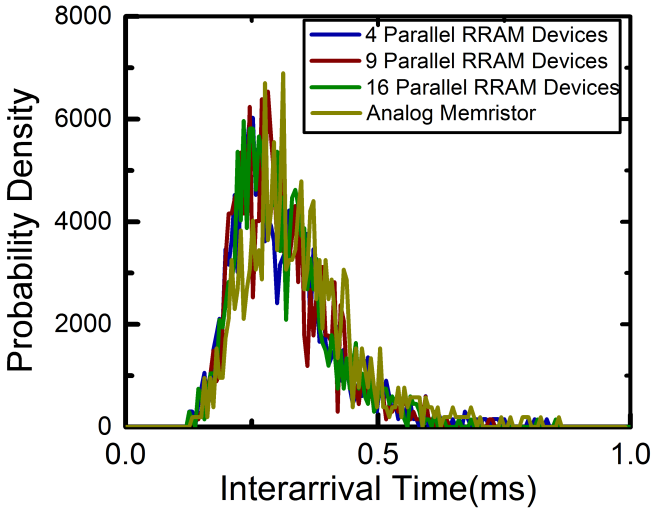



Fig. 9. Probability density of inter-arrival time of the spikes in the output neuron for a synapse made of a single analog memristor and $4, 9$ and 16 discrete RRAM devices. The plot depicts the similarity of the inter-arrival processes related to the spiking in the output neuron.

The average synaptic strength of the group of synapses is already shown in Figure 7 for the two schemes. The standard deviation in the normalized conductance $(G/G_{MAX})$ of the group of 100 synapses varies within a small range (shown as dotted lines in Figure 7) in each case. Since the stimulus applied to the input neurons are all independent and random, and the mean conductivity of all the synapses varies in this small interval, the distribution of inter-arrival time of the post-synaptic stimulus should have a peak around the mean inter-arrival time with sharply trailing edges. Figure 9 shows the probability density distribution of inter-arrival time of the post-synaptic stimulus. As is evident, the distribution of inter-arrival times of the post-synaptic spikes for the analog

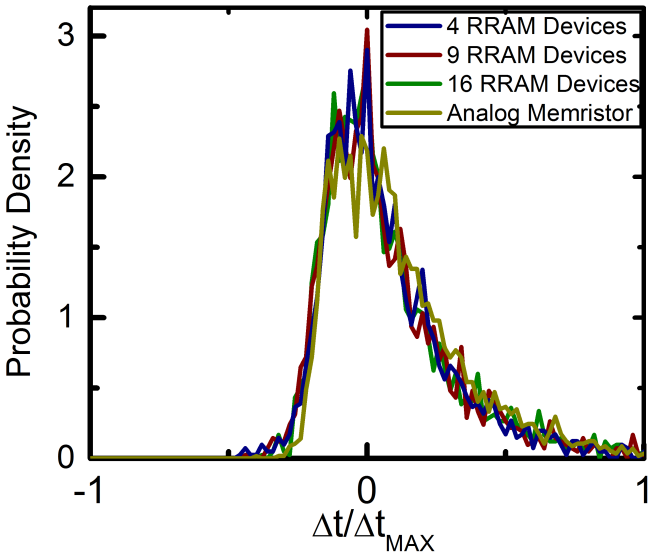



Fig. 10. Probability density of the delay ($\triangle t$) between spikes of the input and output neurons (pre-synaptic to post-synaptic firing delay) with analog memristive synapse and discrete RRAM synapse. The probability density distribution in all the cases is almost identical, ensuring that all the synapses see a similar distribution of pre-synaptic to post-synaptic firing delay. $\Delta t_{MAX} = 1.6\,\text{ms}$.

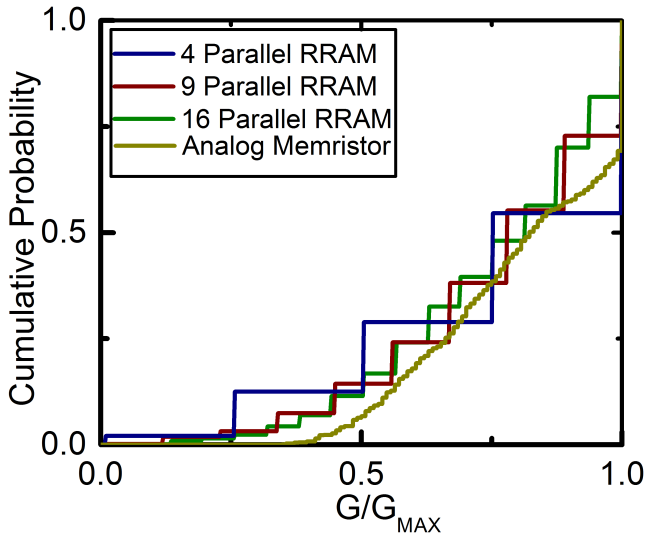



Fig. 11. Cumulative probability of the conductance of a synapse over time for analog and discrete RRAM synapses. In each of these cases, the value of $G/G_{MAX}$ remains below 0.5 for $10-15\%$ of the total time. The approximately identical distribution of $G/G_{MAX}$ ensures almost identical distribution of inter-arrival time of the post-synaptic spikes.

memristive device and the parallel combination of discrete switching devices are statistically almost identical.

Another important statistical property is the probability density distribution of the time interval ($\triangle t$) between pre-synaptic and post-synaptic spike. This was also seen to be statistically almost identical for both types of synapse (Synapse consisting of an analog memristor and a synapse consisting of $k$ parallel RRAM devices) in Figure 10. For all these statistical simulations, the input neurons were stimulated at a rate of $2600\,\text{s}^{-1}$.

Figure 11 shows the distribution of conductance of a synapse over time. Our main intention was to make the effective on-off conductance ratio of the device 2; this implies that the value of normalized synaptic strength (conductance) should be confined ideally between 1 and 0.5. However, in each case of Figure 11 the value of $G/G_{MAX}$ of the device stays below 0.5 for about $10-15\%$ of the total time. This value can however be reduced by further reducing the maximum RESET probability of the RRAM devices.

The distribution of $\triangle G/min(G_{Initial}, G_{Final})$ was also found to be almost identical in all the four cases with the peaks at 0 and sharply trailing edges (Figure 12). This shows that as the number of RRAM devices within the synapse are increased, the device behavior closely mimics that of the analog memristive device.

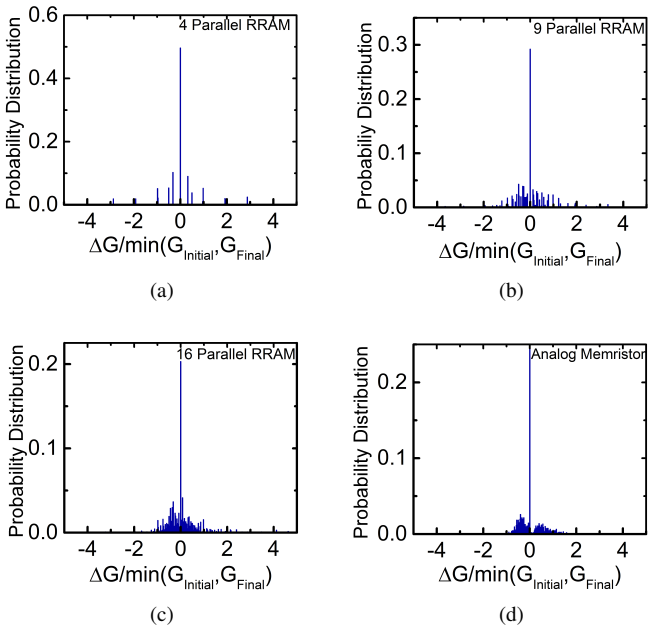



Fig. 12. Probability density of $\triangle G/min(G_{Initial}, G_{Final})$ for a synaptic device consisting of (a) 4 parallel RRAM (b) 9 parallel RRAM (c) 16 parallel RRAM, and (d) a single analog memristor. This plot depicts that the statistical variation of the synaptic conductance shows a similar distribution among the four different schemes. Each of the graphs has a peak at 0 with sharply trailing edges on each side.

## VI. Conclusions

In this paper, we have shown two schemes to implement adaptive synapses in artificial learning systems and proposed a scheme to mimic the analog memristive time dependent learning using a small set (9 or 16) of discrete nanoscale RRAM devices whose switching voltages vary stochastically [12]. Both schemes not only capture spike timing dependent plasticity (STDP) behavior but are also flexible in maintaining a desired on-off ratio of synaptic strength. In addition, the two schemes are almost statistically identical. The demonstrated statistical similarity allows the use of either schemes based on other trade-offs between ease of fabrication and area efficiency.

## REFERENCES


[1] "NAE grand challenges (www.engineeringchallenges.org)."

[2] Bi, Guo-qiang and Mu-ming Poo, "Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type," *The Journal of Neuroscience*, vol. 18, no. 24, pp. 10 464–10 472, 1998.

[3] B. Rajendran, Y. Liu, J. sun Seo, K. Gopalakrishnan, L. Chang, D. Friedman, and M. Ritter, "Specifications of nanoscale devices and circuits for neuromorphic computational systems," *Electron Devices, IEEE Transactions on*, vol. 60, no. 1, pp. 246–253, 2013.

[4] J. Joshua Yang, Matthew D. Pickett, Xuema Li, Douglas A. A. Ohlberg, Duncan R. Stewart and R. Stanley Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature Nanotechnology*, vol. 101, no. 11, pp. 429 – 433, 2008.

[5] L. Chua, "Memristor-the missing circuit element," *Circuit Theory, IEEE Transactions on*, vol. 18, no. 5, pp. 507–519, 1971.

[6] M. Pickett, D. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. Williams, "Switching dynamics in titanium dioxide memristive devices," *Journal of Applied Physics*, vol. 106, no. 7, pp. 074 508–074 508–6, 2009.

[7] B. L. Jackson, B. Rajendran, G. S. Corrado, M. Breitwisch, G. W. Burr, R. Cheek, K. Gopalakrishnan, S. Raoux, C. T. Rettner, A. Padilla, A. G. Schrott, R. S. Shenoy, B. N. Kurdi, C. H. Lam, and D. S. Modha, "Nanoscale electronic synapses using phase change devices," *J. Emerg. Technol. Comput. Syst.*, vol. 9, no. 2, pp. 12:1–12:20, May 2013.

[8] T. Serrano-Gotarredona, T. Masquelier, T. Prodromakis, G. Indiveri, and B. Linares-Barranco, "STDP and STDP variations with memristors for spiking neuromorphic learning systems," *Frontiers in Neuroscience*, vol. 7, no. 2, 2013.

[9] Greg S. Snider, "Spike-timing-dependent learning in memristive nanodevices," in *Nanoscale Architectures, 2008. NANOARCH 2008. IEEE International Symposium on*, June 2008, pp. 85–92.

[10] I. Ebong and P. Mazumder, "Memristor based STDP learning network for position detection," in *Microelectronics (ICM), 2010 International Conference on*, Dec 2010, pp. 292–295.

[11] A. Williamson, L. Schumann, L. Hiller, F. Klefenz, I. Hoerselmann, P. Husar, and A. Schober, "Synaptic behavior and STDP of asymmetric nanoscale memristors in biohybrid systems," *Nanoscale*, vol. 5, pp. 7297–7303, 2013.

[12] B. Long, Y. Li, S. Mandal, R. Jha, and K. Leedy, "Switching dynamics and charge transport studies of resistive random access memory devices," *Applied Physics Letters*, vol. 101, no. 11, 2012.

[13] H. Markram, J. Lübke, M. Frotscher, and B. Sakmann, "Regulation of synaptic efficacy by coincidence of postsynaptic APs and EPSPs," *Science*, vol. 275, pp. 213–215, 1997.

[14] A. Ascoli, F. Corinto, V. Senger, and R. Tetzlaff, "Memristor model comparison," *Circuits and Systems Magazine, IEEE*, vol. 13, no. 2, pp. 89–105, 2013.

[15] Dmitri B. Strukov, Gregory S. Snider, Duncan R. Stewart and R. Stanley Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, 2008.

[16] J. G. Simmons, "Electric tunnel effect between dissimilar electrodes separated by a thin insulating film," *Journal of Applied Physics*, vol. 34, no. 9, 1963.

[17] Kuan-Liang Lin, Tuo-Hung Hou, Jiann Shieh, Jun-Hung Lin, Cheng-Tung Chou and Yao-Jen Lee, "Electrode dependence of filament formation in $HfO_2$ resistive-switching memory," *Journal of Applied Physics*, vol. 109, no. 8, 2011.

[18] A. Chen, "Area and thickness scaling of forming voltage of resistive switching memories," *Electron Device Letters, IEEE*, no. 1, pp. 57–59, 2014.

[19] Branden Long, Yibo Li, and Rashmi Jha, "Switching characteristics of Ru/$Hfo_2$/$TiO_{2-x}$/Ru RRAM devices for digital and analog non-volatile memory applications," *IEEE Electron Device Letters*, vol. 33, no. 5, 2012.

[20] W. Senn and S. Fusi, "Convergence of stochastic learning in perceptrons with binary synapses," *Phys. Rev. E*, vol. 71, p. 061907, Jun 2005.

[21] M. Suri, D. Querlioz, O. Bichler, G. Palma, E. Vianello, D. Vuillaume, C. Gamrat, and B. DeSalvo, "Bio-inspired stochastic computing using binary CBRAM synapses," *Electron Devices, IEEE Transactions on*, vol. 60, no. 7, pp. 2402–2409, July 2013.

[22] Shimeng Yu, Bin Gao, Zheng Fang, Hongyu Yu, Jinfeng Kang, H.S. Philip Wong, "Stochastic learning in oxide binary synaptic device for neuromorphic computing," *Frontiers in Neuroscience*, vol. 7, 2013.

[23] S. Yu, X. Guan, and H. S. P. Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, monte carlo simulation, and experimental characterization," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, Dec 2011, pp. 17.3.1–17.3.4.

[24] Zi-Jheng Liu, Jen-Chun Chou, Shih-Yuan Wei, Jon-Yiew Gan, Tri-Rung Yew, "Improved resistive switching of textured ZnO thin films grown on Ru electrodes," *Electron Device Letters, IEEE*, vol. 32, no. 12, pp. 1728–1730, 2011.

[25] Venkatakrishnan Sriraman, Zhixian Chen, Xiang Li, Xinpeng Wang, Navab Singh, "$HfO_2$ based resistive switching non-volatile memory (RRAM) and its potential for embedded applications," in *2012 International Conference on Solid-State and Integrated Circuit (ICSIC 2012)*, 2012.