2014 International Joint Conference on Neural Networks (IJCNN)
July 6-11, 2014, Beijing, China

Ferroelectric tunnel memristor-based neuromorphic network with 1T1R crossbar architecture

Zhaohao Wang, Weisheng Zhao*, Wang Kang, Youguang Zhang,
Jacques-Olivier Klein, and Claude Chappert

***Abstract*—Emerging ferroelectric tunnel memristors show large OFF/ON resistance ratio (>100) and high operation speed (~10ns), promising to be widely applied in the future synapse-like systems. In this paper we propose a neuromorphic network with ferroelectric tunnel memristor. This network is arranged with classical crossbar topology, in which each crosspoint forms a synapse consisting of a MOS transistor and a memristor. Based on this architecture, we design a spike-timing dependent plasticity (STDP) scheme and a parallel supervised learning circuit. Using a compact model of ferroelectric tunnel memristor and CMOS 40nm design kit, we perform transient simulation to validate the functionality of the proposed STDP and learning circuit. Simulation results show the potential of our neuromorphic network in low power (~100nA or ~1μA) and high speed (~1μs or ~100ns) computing system.**

I. Introduction

MEMRISTOR is an emerging electronic element whose conductance can be tuned with the history of voltage applied across it or current flowing through it [1]–[2]. Discovery of memristor [2] has recently driven numerous researches in a variety of applications such as memory [3], logic block [4], and neuromorphic network [5]. Among them, neuromorphic network is showing great potential in the next generation computing system. As shown in Fig. 1, neuromorphic network is composed of neurons responsible for processing inputs and synapses connecting the inputs and neurons. Input signals are weighted by synapses and then are integrated and activated by neurons. In this scenario the tunable conductance of memristor can be naturally used as synaptic weight (see Fig. 2a). Memristor-based neuromorphic network provides two main advantages over conventional computing systems: first, thanks to tunable conductance of memristor, the neuromorphic systems are highly tolerant to device variations and defects originating from nanoscale fabrication technology. Second, non-volatility of memristors promises to overcome the energy and delay bottleneck suffered by traditional von Neumann computing system. Therefore intensive research efforts are being dedicated to this field and neuromorphic systems based on various memristors [6]–[12] have been proposed.

Z. H. Wang, W. S. Zhao, J.-O. Klein and C. Chappert are with the Institut d'Electronique Fondamentale (IEF), CNRS UMR 8622, Université Paris-Sud XI, 91405 Orsay, France (e-mail: weisheng.zhao@u-psud.fr, and zhaohao.wang@u-psud.fr).

W. Kang and Y. G. Zhang are with the department of Electrical Engineering, Beihang University, 100191, Beijing, China.

This work was supported by the French project ANR-MARS, PEPS-NVCPU and CSC.

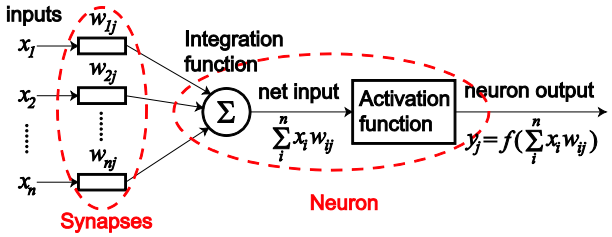

Fig. 1 Schematic diagram of a neuromorphic network composed of *n* inputs, *n* synapses and a single neuron.

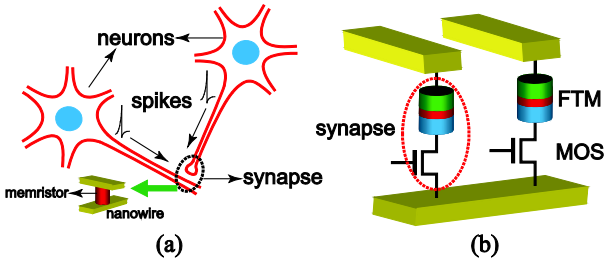

Fig. 2 (a) Nanoscale memristor can be used as synapse for connecting neurons and weighing input spikes. (b) The proposed network architecture in this paper, where a synapse is composed of a memristor and a connected MOS transistor.

In this paper we employ a novel type of memristor, ferroelectric tunnel memristor (FTM), to build neuromorphic network. FTMs have been experimentally demonstrated by many research groups with different fabrication technologies [13]–[17]. Among them the memristor reported in [13] is used in our research because it shows large OFF/ON resistance ratio (>100) and high operation speed (~10ns). We design a neuromorphic network based on crossbar topology, in which the FTM is connected in series with an MOS transistor to form a 1T1R synapse at each crosspoint (see Fig. 2b). The 1T1R structure can relieve the sneak path problem [18] and incorrect programming induced by noise, because the external programming signal can be securely cut off by controlling the gate voltage of MOS transistor. In addition, crossbar topology allows high density integration and parallel computing. We proposed two applications for this neuromorphic network: spike-timing dependent plasticity (STDP) and parallel supervised learning. With a compact model of FTM and CMOS 40nm design kit [19], we performed transient simulation to validate these two applications.

The rest of this paper is organized as follows: in the next section, we briefly introduce the working principle and compact model of FTM. In section III, we propose a STDP scheme and demonstrate corresponding simulation results. In

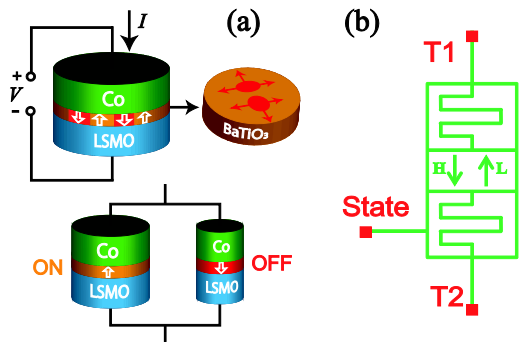

Fig. 3 (a) The structure of $Co/BaTiO_3/La_{0.67}Sr_{0.33}MnO_3$ FTM and its equivalent model of resistance based on ferroelectric switching dynamics: Once a programming voltage is applied to the ferroelectric film with fully up-polarized domain (orange), the down-polarized domains (red) nucleate and propagate, and hence the tunnel resistance is calculated by the parallel resistance model. (b) Model symbol of FTM under *Spectre* simulator.

section IV, a parallel supervised learning circuit is designed and simulated based on our neuromorphic network. Finally we provide conclusion and prospective in section V.

II. FTM and Its Compact Model

The structure and working principle of the FTM is schematically shown in Fig. 3a, where a ferroelectric ultrathin barrier ($BaTiO_3$) is sandwiched between two different electrodes (Co and $La_{0.67}Sr_{0.33}MnO_3$). The ferroelectric barrier has a spontaneous polarization which can be switched between upward and downward by applying a programming voltage. This polarization switching causes the modulation of barrier potential profile [20]–[22], and hence tunnel resistance changes between ON and OFF states. Recently experimental observations [13], [15] indicated that ferroelectric polarization is switched region-by-region rather than abruptly, in other words, the switching is a process of ferroelectric domain growth including nucleation and subsequent domain wall propagation. Therefore polarization switching can be controlled to reach intermediate state where the up-polarized and down-polarized domains coexist in ferroelectric barrier (see Fig. 3a). In such a case, the resistance of FTM (or memristance, R_M) is equivalent to the parallel resistance of two FTMs associated with ON and OFF states, respectively:

$$\frac{1}{R_M}=\frac{s_{ON}}{R_{ON}}+\frac{s_{OFF}}{R_{OFF}} \tag{1}$$

where R_{ON} and R_{OFF} are the resistances of ON state (when the barrier is fully up-polarized) and OFF state (when the barrier is fully down-polarized), respectively, s_{ON} and s_{OFF} are volume fractions of up-polarized and down-polarized domains, respectively, and $s_{ON}+s_{OFF}=1$.

We have recently developed a compact model for this FTM based on physical theories and experimental results [23]–[24]. In this model, the growth of ferroelectric domain is described by classical KAI model [25]–[26]. We choose volume fraction of down-polarized domain (denoted by s) as state variable to define this voltage-controlled FTM, as (2) and (3)

TABLE I
Main Parameters for Compact Model[1]

Parameter	Description	Default value
t_{BTO}	BTO film thickness	2nm
$Area$	Tunnel junction area	π×175nm×175nm
$R_{ON}{\cdot}Area$	Resistance-area product for ON state	15.525kΩ·μm^2 (Read voltage: 100mV)
$R_{OFF}{\cdot}Area$	Resistance-area product for OFF state	4.44MΩ·μm^2 (Read voltage: 100mV)
τ_N	Nucleation time	7.47ns (Write voltage: 3.5V)
τ_P	Characteristic propagation time	8.75ns (Write voltage: 3.5V)

[1] Corresponding to experimental measurements in [13].

$$V(t)=R(s,V)I(t)=\frac{1}{\left[1-s(t,V)\right]/R_{ON}+s(t,V)/R_{OFF}}I(t),\ t>\tau_N \tag{2}$$

$$\frac{ds}{dt}=f(s,V)=(1-s)\frac{2}{\tau_P(V)}\sqrt{\ln\left(\frac{1}{1-s}\right)} \tag{3}$$

where τ_N and τ_P are nucleation time and characteristic propagation time, respectively. Both of them are voltage-dependent functions. Equation (2) indicates that memristive behaviour occurs only after a delay of τ_N (i.e. nucleation is achieved), because the propagation of domain is not activated during $t<\tau_N$.

A low complexity algorithm is developed to resolving s at given initial values (s_0, t_0) and V, as (4) and (5)

$$t_r=\tau_P(V)\cdot\sqrt{\ln\left(\frac{1}{1-s_0}\right)} \tag{4}$$

$$s(t_0+\Delta t,V)=1-\exp\left\{-\left[\frac{t_r+\Delta t}{\tau_P(V)}\right]^2\right\} \tag{5}$$

where Δt is time step of simulation. The calculation of other parameters (e.g. τ_N, τ_P, R_{ON}, R_{OFF}) is presented in [23]–[24].

These numerical models have been programmed with Verilog-A language and integrated together on Cadence platform. Fig. 3b shows the model symbol under Spectre simulator. Three pins are designed for this symbol: T1 and T2 are physical pins corresponding to two electrodes (Co and $La_{0.67}Sr_{0.33}MnO_3$). "State" is a virtual pin for monitoring the volume fraction of down-polarized domain. It outputs a voltage ranging from 0V (corresponding to volume fraction = 0%) to 1V (corresponding to volume fraction = 100%). Two arrows ("H" and "L") indicate the polarities of applied pulse required to activate the growth of down-polarized and up-polarized domain, respectively.

The accuracy of this model has been validated by relative good agreement between simulation results and experimental measurement [23]. Fig. 4 shows a single-cell transient simulation of this model. The main parameters are set to

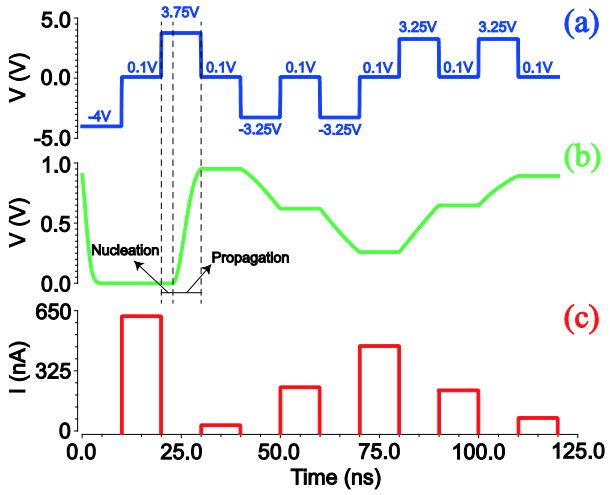

Fig. 4 A single-cell transient simulation with compact model. (a) The waveform of applied pulse. (b) The voltage of "State" pin, which indicates the growth of down-polarized domain. (c) The current measured at 0.1V.

default value as Table I. In this example, we applied several programming pulses, each of which is followed by a small read pulse of 0.1V (see Fig. 4a). During 0~20ns of simulation, a negative voltage (−4V) sets FTM to ON state, which means volume fraction of down-polarized domain is nearly zero, in agreement with simulation results in Fig. 4b. Afterwards, during 20~40ns, a positive voltage (3.75V) activates the growth of down-polarized domain, meanwhile processes of domain nucleation and propagation can be observed in Fig. 4b. Finally, during 40ns~120ns, we applied two negative pulses (−3.25V) and two positive pulses (3.25V) to program FTM successively, during this period volume fraction of down-polarized domain decreases or increases depending on the polarity of applied voltage, as shown in Fig. 4b. During the entire simulation, the resistance changes with growth of domain, which are verified by simulation results in Fig. 4c.

III. Implementation of STDP in FTM-based Neuromorphic Network

STDP is an unsupervised learning mechanism that emulates the synaptic response between neurons in mammalian brains [27]–[28]. Neuroscience reveals that the strength of connection between neurons is characterized by the magnitude of synaptic efficacy (or weight). Experimental results of STDP proved that synaptic weight is tuned depending on the timing of pre-neuron and post-neuron spikes ($\Delta t = t_{pre} - t_{post}$, where pre-neuron spikes at t_{pre} and post-neuron spikes at t_{post}). If the pre-neuron spikes before the post-neuron ($\Delta t > 0$), synaptic weight increases ($\Delta\omega > 0$) and this process is called long-term potentiation (LTP), otherwise ($\Delta t < 0$) synaptic weight decreases ($\Delta\omega < 0$) and long-term depression (LTD) occurs. Experimental data [28] suggest that $\Delta\omega$ is approximately exponential function of Δt.

A. Network architecture and operation

We design a STDP scheme for FTM-based neuromorphic network by referring to ideas in [6], [29]–[30]. The connection between 1T1R synapse and neurons is shown in Fig. 5a. It is seen that pre-neuron communicates with post-neuron by a current flowing through FTM and transistor. During the operation, pre-spike is applied to gate of transistor, while post-spike is applied to top electrode of FTM (TE) and source electrode of transistor (BE).

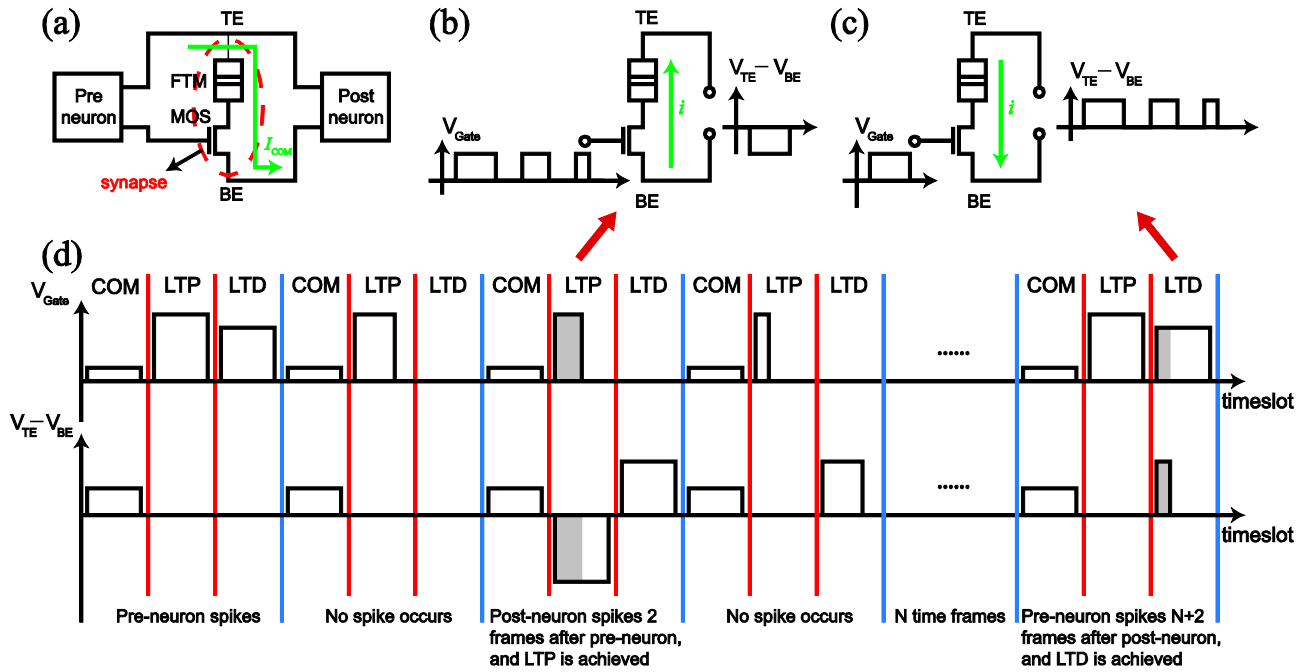

Fig. 5 (a) Schematic illustration of 1T1R synapse between pre-neuron and post-neuron. The synapse (red) and communication current (green) are marked, respectively. (b) ~ (c) The realization of LTP (b) and LTD (c) in the proposed STDP scheme. It is seen that overlap of spikes produces programming voltage of two polarities on FTM. Then the FTM conductance is tuned depending on the width of programming pulse. (d) The diagram of detailed time sequence describing the working flow of STDP scheme.

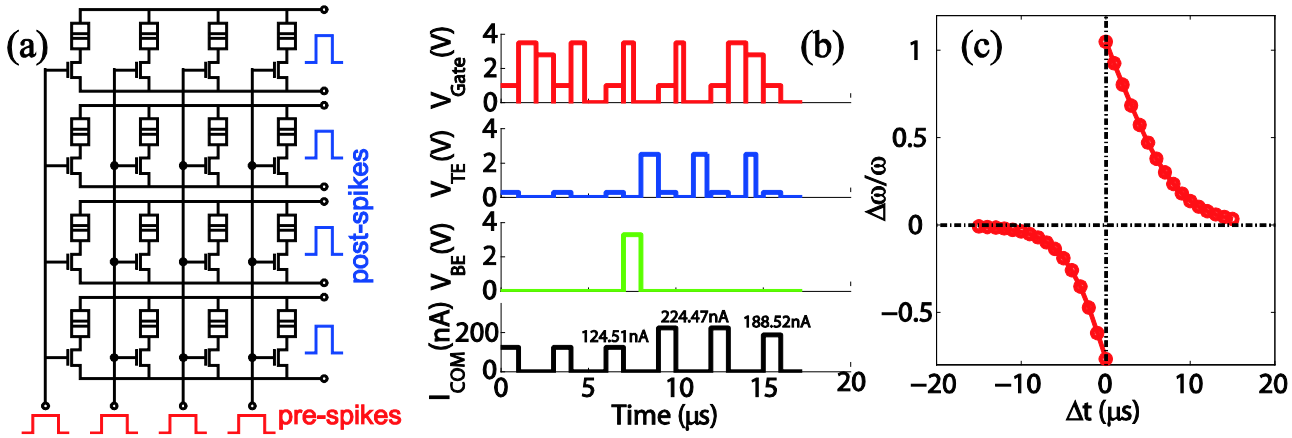

Fig. 6 (a) The 4×4 crossbar neuromorphic network for STDP simulation. (b) The signal sequences of V_{Gate}, V_{TE}, V_{BE} and I_{COM} in a simulation example. (c) The measured change of synaptic weight as a function of relative timing of neuron spikes.

TABLE II
PARAMETERS FOR STDP SIMULATION

Parameter description	Value
Tunnel junction area	π×100nm×100nm
Initial volume fraction of down-polarized domain	90%
MOS transistor channel width/length	0.5μm/1.2μm
V_{Gate}	Communication: 1V LTP/LTD: 3.5V/2.8V
V_{TE}-V_{BE}	Communication: 0.3V LTP/LTD: -3.3V/2.5V
Duration of timeslot	1μs

In our scheme, time division multiplexing (TDM) is used to organize the operation. The working flow and signal settings are illustrated in Fig. 5d. One time frame is composed of three time slots: communication, LTP and LTD. In the communication timeslot, the pre-neuron produces a spike signal on MOS gate while a read voltage (V_{TE}−V_{BE}) is applied between TE and BE, as a result a current (I_{COM}) flowing from pre-neuron to post-neuron. The synaptic weight is measured by $\omega = I_{COM}/(V_{TE}-V_{BE})$. During the communication, the state of FTM is required to keep unaffected, therefore the read voltage is set to low amplitude to avoid the unexpected programming to FTM.

In the LTP timeslot, a positive pulse whose width decays with the time frame is generated at the MOS gate when pre-neuron spikes. Meanwhile, a negative pulse of constant width is triggered between the TE and BE when post-neuron spikes. Unlike pre-spike, this negative pulse (post-spike) lasts for only one timeslot. Only when post-neuron spikes after the pre-neuron, the MOS gate is activated and the FTM can be programmed by the negative pulse from pre-neuron (see Figs. 5b and 5d). In other words, time difference between pre-spike and post-spike is translated into the width of programming pulse. Similarly, in the LTD timeslot, post-spike causes a positive pulse of decaying width between TE and BE while pre-spike produces a positive pulse of constant width at MOS gate for only one timeslot (see Figs. 5c and 5d). In LTP/LTD timeslot, the pulses are adjusted to appropriate amplitude to generate desired programming signal to FTM.

It is seen that two spiking signals (V_{Gate} and V_{TE}−V_{BE}) from pre-neuron and post-neuron are required simultaneously to activate the LTP/LTD process. Therefore this scheme eliminates the interference among synapses (e.g. sneak path problem [18]) in crossbar architecture since single spike are not able to program the FTM.

B. *Simulation and validation*

The proposed STDP scheme was simulated with compact model of FTM and CMOS 40nm design kit [19] on Cadence *Spectre* simulator. We designed a 4×4 crossbar network shown in Fig. 6a as simulation environment. The pulse of decaying width can be produced by the pulse width modulation (PWM) block. The main parameters are configured as Table II, and one simulation example is shown in Fig. 6b.

In Fig. 6b, at the first frame the pre-neuron spikes (0~3μs), after two frames a post-spike occurs and activates LTP (6~9μs), i.e. the current (I_{COM}) flowing through synapse increases from 124.51nA to 224.47nA. Similarly, pre-neuron spikes once again 2 frames later (12~15μs). Then LTD is achieved and I_{COM} decreases from 224.47nA to 188.52nA. Since the read voltage is fixed to a constant, the change of I_{COM} means the modulation of synaptic weight controlled by neuron spikes.

In order to validate the proposed STDP scheme, we measured the change of synaptic weight (I_{COM}/0.3V) versus the time difference between post-spike and pre-spike. Corresponding simulation results are summarized and shown in Fig. 6c. It is seen that the change of synaptic weight increases exponentially with the time difference vanishing, in good agreement with experimental measurement [28].

IV. FTM-BASED PARALLEL SUPERVISED LEARNING CIRCUIT

The crossbar topology supports high density integration and parallel operation, which can save area and delay overhead. Based on this advantage, we developed a parallel supervised learning circuit for proposed FTM-based neuromorphic network.

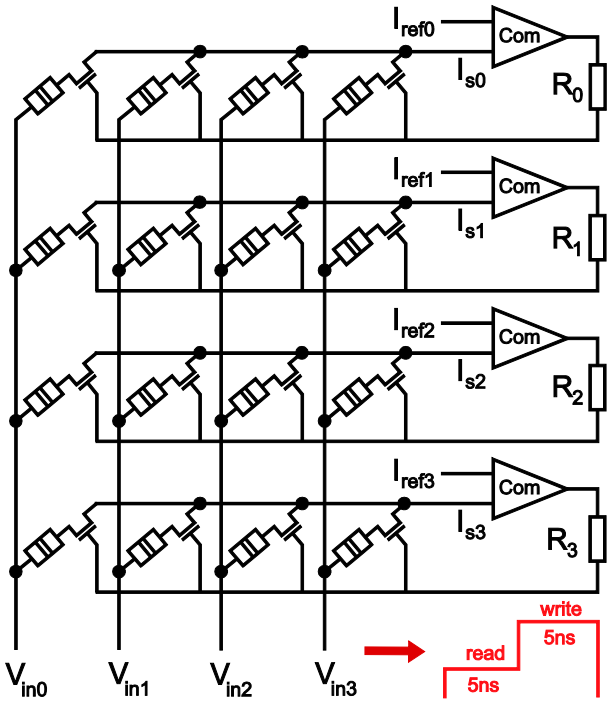

Fig. 7 The architecture of parallel supervised learning circuit based on 4×4 crossbar topology. R_0~R_3 are set to 10kΩ for mitigating the signal oscillation. Inset shows the waveform of input signal applied to V_{in0} ~V_{in3}.

A. Circuit design

The parallel supervised learning circuit is designed based on our previous work [31], as shown schematically in Fig. 7. In this configuration, all synapses within the same row share the same gate and source electrode of MOS transistor. They are used as feedback control and output, respectively. FTM electrodes within the same column are connected together and carry the input signals of pre-neurons. A current comparator serves as post-neuron in each row. It accumulates the currents flowing through the synapses associated with inputs and compares them with reference values to be targeted. The output of comparator is connected with the MOS gates within the same row to form the feedback loop.

For a set of inputs, the goal of learning is to configure synapse array so that the expected current ($I_{ref0\sim3}$ in Fig. 7) can be obtained in the post-neuron. Learning process is composed of initialization and learning phases. During the initialization phase, all FTMs are programmed to the largest conductance. Learning phase includes read and write operations, as shown in the pulse signal of Fig. 7. During the read operation, the post-neuron (current comparator) in each row accumulates the input current ($I_{s0\sim3}$ in Fig. 7) weighted by synapses and compares it with expected current. Subsequently, during the write operation, depending on the error between two currents, post-neuron adjusts the FTM conductance by applying a positive voltage to shared MOS gate. Once the expected current is reached, post-neuron generates a negative voltage to close the shared MOS gate, and the expected current is maintained until all rows achieve learning.

Importantly, the learning process of this circuit is performed in a parallel way. Therefore the learning delay is the largest duration of learning phase spent by one row, rather than total duration of all branches like conventional serial schemes. This feature improves significantly the throughput of neuromorphic network.

TABLE III
PARAMETERS FOR SIMULATION OF LEARNING CIRCUIT

Parameter description	Value
Tunnel junction area	π×80nm×80nm
Programming voltage	4.5V
MOS transistor channel width/length	0.5μm/1.2μm
Read voltage	(0.3V, 0.4V, 0.5V, 0.6V) for (V_{in0}, V_{in1}, V_{in2}, V_{in3})
Targeted values	(9μA, 8μA, 7μA, 6μA) for (I_{s0}, I_{s1}, I_{s2}, I_{s3})
Period of input signal	10ns : write voltage of 5ns followed by read voltage of 5ns

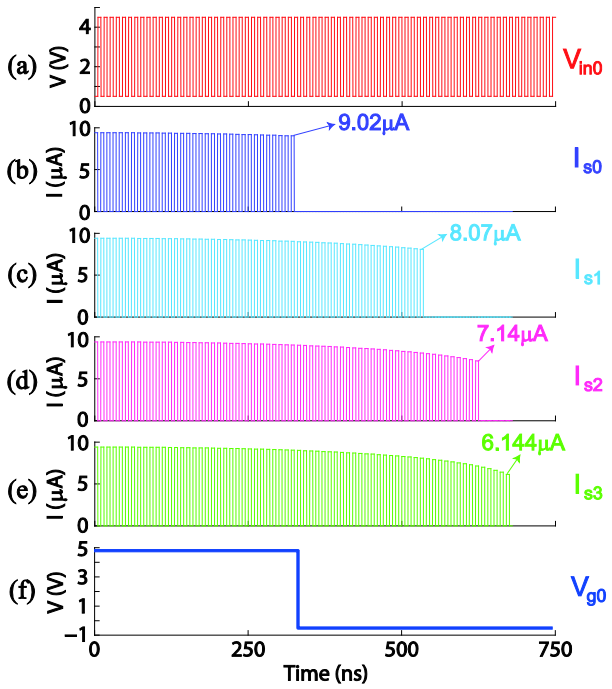

Fig. 8 The transient simulation of learning circuit. (a) The input voltage applied to V_{in0}. (b) ~ (e) The evolution of read currents during learning phase for I_{s0} ~ I_{s3}. (f) The feedback signal applied to V_{g0}.

B. Simulation results

We performed transient simulation of this learning circuit with aforementioned compact model and design kit. The main simulation parameters are configured as Table III. Simulation results of learning phase is shown in Fig. 8, where the adjustment of accumulative currents ($I_{s0\sim3}$) is demonstrated. Since all of FTMs are set to the same conductance during the initialization phase, the current is adjusted from the identical initial value (9.402μA in Fig. 8b ~ 8e). Depending on the magnitude of targeted current, each row achieves learning process after a specific delay. Fig. 8f demonstrates that a negative pulse is sent to the shared MOS gate when targeted current of I_{s0} is reached. Finally all learnt currents are close to expected values and thus the learning circuit is validated.

V. Conclusion and Prospective

We have proposed a 1T1R crossbar neuromorphic network with emerging ferroelectric tunnel memristor. A spike-timing dependent plasticity scheme and a parallel supervised learning circuit were designed as typical applications of proposed network. With a compact model of FTM and CMOS 40nm design kit, we performed transient simulation to validate these two applications. Simulation results show low current (~100nA or ~1μA) and low delay (~1μs or ~100ns), confirming great potential of this architecture in low power and high speed computing system. Nevertheless, there are still issues to explore in optimization of performance. Typically, the programming voltage of FTM can be further decreased to improve the compatibility with nanoscale CMOS technology [32]. Some efforts, such as replacing $BaTiO_3$ with other ferroelectric material and exploring advanced fabrication technology, are under the investigation.

Acknowledgment

The authors thank to A. Chanthbouala, S. Boyn, M. Bibes and J. Grollier for fruitful discussions.

References

[1] L. O. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, pp. 507–519, Sep. 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, May 2008.

[3] Y. Ho, G. M. Huang, and P. Li, "Nonvolatile memristor memory: device characteristics and design implications," in *Proc. IEEE Int. Conf. Computer-Aided Design*, San Jose, 2009, pp. 485–490.

[4] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart and R. S. Williams, "'Memristive'switches enable 'stateful'logic operations via material implication," *Nature*, vol. 464, pp. 873–876, Apr. 2010.

[5] D. Kuzum, S. Yu, and H. S. P. Wong, "Synaptic electronics: materials, devices and applications," *Nanotechnology*, vol. 24, pp. 382001, Sep. 2013.

[6] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviy, P. Mazumder and W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," *Nano Lett.*, vol. 10, pp. 1297–1301, Mar. 2010.

[7] D. Kuzum, R. G. D. Jeyasingh, B. Lee, and H. S. P. Wong, "Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing," *Nano Lett.*, vol. 12, pp. 2179–2186, Jun. 2011.

[8] T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski and M. Aono, "Short-term plasticity and long-term potentiation mimicked in single inorganic synapses," *Nature Mater.*, vol. 10, pp. 591–595, Aug. 2011.

[9] F. Alibart, E. Zamanidoost and D. B. Strukov, "Pattern classification by memristive crossbar circuits using ex situ and in situ training," *Nature Commun.*, vol. 4, Jun. 2013.

[10] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Netw.*, vol. 23, pp. 881–886, Sep. 2010.

[11] O. Bichler, W. S. Zhao, F. Alibart, S. Pleutin, S. Lenfant, D. Vuillaume *et al.* "Pavlov's dog associative learning demonstrated on synaptic-like organic transistors," *Neural Comput.*, vol. 25, pp. 549–566, Sep. 2012.

[12] S. Y. Liao, J. M. Retrouvey, G. Agnus, W. S. Zhao, C. Maneux, S. Fregonese *et al.* "Design and modeling of a neuro-inspired learning circuit using nanotube-based memory devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, pp. 2172–2181, Sep. 2011.

[13] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya *et al.* "A ferroelectric memristor," *Nature Mater.*, vol. 11, pp. 860–864, Oct. 2012.

[14] D. J. Kim, H. Lu, S. Ryu, C-W. Bark, C-B. Eom, E. Y. Tsymbal, and A. Gruverman, "Ferroelectric tunnel memristor," *Nano Lett.*, vol. 12, pp. 5697–5702, Oct. 2012.

[15] H. Yamada, V. Garcia, S. Fusil, S. Boyn, M. Marinova, A. Gloter *et al.* "Giant electroresistance of super-tetragonal $BiFeO_3$–based ferroelectric tunnel junctions," *ACS nano*, vol. 7, pp. 5385–5390, May 2013.

[16] Z. Wen, C. Li, D. Wu, A. Li, and N. Ming, "Ferroelectric-field -effect-enhanced electroresistance in metal/ferroelectric/semiconductor tunnel junctions," Nature Mater., vol. 12, pp. 617–621, Jul. 2013

[17] Z. Hu, Q. Li, M. Li, Q. Wang, Y. Zhu, X. Liu, *et al.* "Ferroelectric memristor based on $Pt/BiFeO_3/Nb$-doped $SrTiO_3$ heterostructure," *Appl. Phys. Lett.*, vol. 102, pp. 102901, Mar. 2013.

[18] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nature Mater.*, vol. 9, no. 5, pp. 403–406, May 2010.

[19] CMOS40 Design Rule Manual (STMicroelectronics, 2012).

[20] E. Y. Tsymbal and H. Kohlstedt, "Tunneling across a ferroelectric," *Science*, vol. 313, pp. 181–183, Jul. 2006.

[21] M. Y. Zhuravlev, R. F. Sabirianov, S. S. Jaswal, and E. Y. Tsymbal, "Giant electroresistance in ferroelectric tunnel junctions," *Phys. Rev. Lett.*, vol. 94, pp. 246802, Jun. 2005.

[22] H. Kohlstedt, N. A. Pertsev, J. Rodriguez Contreras, and R. Waser, "Theoretical current–voltage characteristics of ferroelectric tunnel junctions," *Phys. Rev. B*, vol. 72, pp. 125341, Sep. 2005.

[23] Z. H. Wang, W. S. Zhao, W. Kang, Y. Zhang, J.-O. Klein *et al.* "Compact modelling of ferroelectric tunnel memristor and its using for neuromorphic simulation," *Appl. Phys. Lett.*, vol. 104, pp. 053505, Feb. 2014.

[24] Z. H. Wang, W. S. Zhao, W. Kang, A. Bouchenak-Khelladi, Y. Zhang, J.-O. Klein *et al.* "A physics-based compact model of ferroelectric tunnel junction for memory and logic design," *J. Phys. D: Appl. Phys.*, vol. 47, pp. 045001, Jan. 2014.

[25] Y. Ishibashi and Y. Takagi, "Note on ferroelectric domain switching," *J. Phys. Soc. Jpn.*, vol. 31, pp. 506–510, Aug. 1971.

[26] S. Hashimoto, H. Orihara, and Y. Ishibashi, "Study on D-E hysteresis loop of TGS based on the Avrami-type model," *J. Phys. Soc. Jpn*, vol. 63, pp. 1601–1610, Apr. 1994.

[27] W. Gerstner, R. Ritz, and J. L. Van Hemmen, "Why spikes? Hebbian learning and retrieval of time-resolved excitation patterns," *Biol. Cybern.*, vol. 69, pp. 503–515, Sep. 1993.

[28] G. Bi and M. Poo, "Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type," J. Neurosci., vol. 18, pp. 10464–10472, Dec. 1998.

[29] S. Ambrogio, S. Balatti, F. Nardi, S. Facchinetti and D. Ielmini, "Spike-timing dependent plasticity in a transistor-selected resistive switching memory," *Nanotechnology*, vol. 24, pp. 384012, Sep. 2013.

[30] G. S. Snider, "Spike-timing-dependent learning in memristive nanodevices," in *IEEE Int. Symp. Nano. Archi.*, Anaheim, 2008, pp 85–92.

[31] W. S. Zhao, G. Agnus, V. Derycke, A. Filoramo, J.-P. Bourgoin and C. Gamrat, "Nanotube devices based crossbar architecture: toward neuromorphic computing," Nanotechnology, vol. 21, pp. 175202, Apr. 2010.

[32] Z. H. Wang, W. S. Zhao, W. Kang, A. Bouchenak-Khelladi, Y. Zhang, J.-O. Klein *et al.* "Write operation study of Co/BTO/LSMO ferroelectric tunnel junction," *J. Appl. Phys.*, vol. 114, pp. 044108, Jul. 2013.