Multi-objective genetic algorithms for reducing mark read-out effort in lithographic tests

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ABSTRACT

This paper describes an application of multi-objective genetic algorithms (MOGA) to an optimization problem in the context of lithographic testing. The overall aim is to find a general procedure for reducing mark read-out effort in lithographic tests with limited degradation of related performance indicators. In these tests, silicon wafers are exposed with marks which are then read-out to determine lithographic performance expressed, for instance, with the 99.7 percentile of the read-out marks.

The problem was solved by applying MOGA in two stages. The first stage aims at determining a reduced layout in which for each field the same marks are read-out. In the second stage, the aim is to determine a reduced layout in which different fields have different marks read-out. In both stages the conflicting objectives are two: the number of read-out marks and the chosen performance indicator.

The recombination and mutation operators applied in MOGA are different in the two stages and are derived from a statistical analysis of the input data.

This approach, when applied to overlay test data, leads to a 50% reduction in read-out marks with 10% degradation range in performance indicators when compared to the full layout.

CCS CONCEPTS

• **Applied computing → Physical sciences and engineering → Engineering → Computer-aided design**;

KEYWORDS

Multi-objective optimization, lithography.

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1 INTRODUCTION

A *lithographic scanner* [1] is a machine used in the manufacturing of integrated circuits (IC). Its way to operate is similar, in principle, to the one of a digital projector (see Figure 1, left side). A *light beam* goes through a semi-transparent support (*reticle* – see Figure 1, right-top side) on which some *patterns* are present. The light beam will reach a *silicon wafer* coated with photoresist: a light sensitive material. This process is called *exposure*. The pattern present on the reticle is reduced in size by a certain factor (through the *reduction lens*) before reaching the wafer. Moreover, this pattern is exposed several times on the same wafer. The portion of a wafer where the pattern of a reticle has been exposed is called *field* (see Figure 1, right-bottom side). A *layer* is the exposure of a reticle on a wafer. ASML scanners have two locations (called *chucks*) where wafers can be placed in order to be exposed. A wafer entering such a scanner can either be exposed while being on chuck 1 or on chuck 2. After exposure, wafers are developed and etched. In this way the pattern present on the reticle is reproduced on each field of the wafer. ICs are created by exposing several layers, with different reticles, on the same wafer.

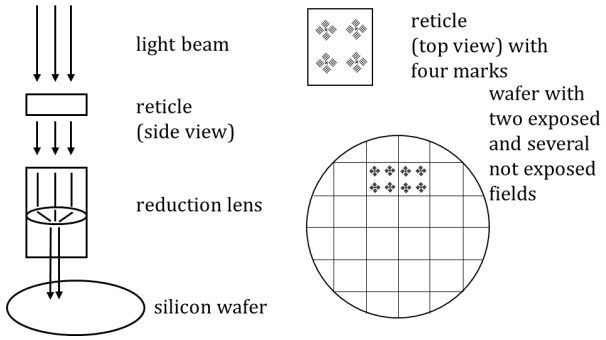

Figure 1: (left side) working principle of a lithographic scanner, (right side) a reticle with marks (top) and a wafer with exposed and not-exposed fields (bottom).

Lithographic scanners are very precise machines. They can superimpose the pattern of one layer on the pattern of the previous

layer with a XY displacement error, known as *overlay*, of at most 2nm.

It takes several weeks to build such a machine. During the build-up of a scanner several tests are performed to calibrate a scanner or verify its performance.

Calibration tests determine the imprecision of a certain aspect of a scanner and they correct for it. *Qualification tests* check if a certain aspect of the scanner is within given specification limits. For instance, some tests measure overlay, others *focus* (the capability of a scanner to keep the image on focus when exposing), etc.

Several of these tests require exposing and reading-out wafers. The patterns in the reticles used in these tests are dedicated *marks* (see Figure 1, right-top side), which can be read-out by appropriate sensors. In an overlay test, the value which is read-out for each mark is the overlay error: the XY displacement between the position a mark was expected to be in and the position the mark really is on a wafer (see Figure 2).

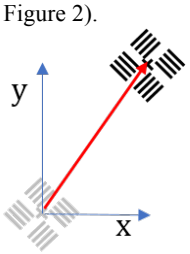

Figure 2: overlay error (red line), with its x and y components, between where the mark is expected to be (gray mark) and where it is (black mark) on a wafer.

Reducing the amount of time needed to read-out test wafers without performance degradation, is of paramount importance both for scanner producers and chip manufacturers. For scanner producers it means less time to complete the manufacturing of scanners; for chip manufacturers it means less time needed to service scanners.

Currently, there is no general procedure available to reduce the number of read-out marks. Normally, all marks are read-out.

2 PROPOSED ALGORITHM

The proposed algorithm consists of 3 steps:

1) Performing statistical analysis on test data to understand sources of variation. The outcome of this step is used to define operators to be used in the 2 subsequent steps;
2) Applying a multi-objective genetic algorithm (MOGA) [2] to find a wafer reduced layout where each field has the same reduced layout;
3) Applying MOGA to find a reduced layout where different fields have different reduced layouts.

This algorithm has been applied to Match Machine Overlay (MMO), an overlay test. In this test 6 wafers are exposed, 3 on chuck 1 and 3 on chuck 2, with 76 fields each. Each field contains 49 marks arranged in 7 columns and 7 rows. A total of 3035 marks fall within a wafer. We consider the mean + 3σ ($m3\sigma$, σ being the standard deviation) for the X and Y displacement of the wafer exposed on chuck 1 (C1) and chuck 2 (C2) as performance indicators for this test. These four objectives are not conflicting. This means that the multi-objective optimization has two objectives: the number of marks and the four m3σ, i.e., two m3σ for chuck 1 (C1 X m3σ, C1 Y m3σ) and two for chuck 2 (C2 X m3σ and C2 Y m3σ). The number of marks conflicts with the other objectives. This is because the less marks one reads-out, the more degradation will result in these performance indicators compared to the full read-out.

We had MMO data for 3 different machines: M1, M2 and M3. We did run our algorithm only on one of these MMO data (coming from M1) and we verified the obtained reduced layout on the two remaining MMO data sets.

Several reduced layouts resulted from this algorithm. This algorithm proved to be very stable to different random seeds. The returned individuals with the same number of marks look different, but they resulted in very similar performance degradations. The performance degradations of different runs were +/- 1% different. Figure 3 shows such a layout with 1591 marks (50.38% of 3035, the number of marks within a wafer when a full layout is employed).

Figure 3 shows the performance degradation induced by this layout. Here the range is 103.228 - 93.7663 = 9.4617.

All in all, this approach, when applied to MMO test data, leads to a 50% reduction in read-out marks with 10% degradation range in performance indicators when compared to the full layout.

This is a viable solution to reduced mark read-out.

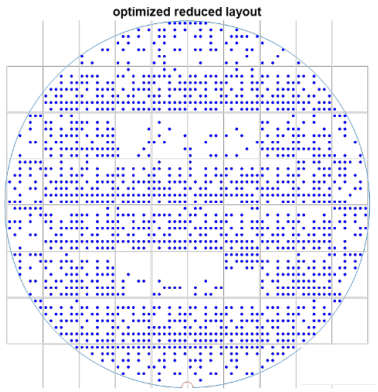

Figure 3: A reduced layout with 1591 marks (blue dots). Marks which are not read-out are not indicated.

Table 1: Performance degradation induced by the layout in Figure 3

	M1	M2	M3
C1 X m3σ	103.1614	100.0965	99.7663
C1 Y m3σ	100.9511	99.7554	93.9518
C2 X m3σ	101.5235	100.1177	95.6884
C2 Y m3σ	102.7116	103.2280	94.4867

REFERENCES

[1] C. Mack, 2012. *Fundamental Principles of Optical Lithography: The Science of Microfabrication*. Wiley, NY, 2012.

[2] K. Deb, 2001. *Multi-objective optimization using evolutionary algorithms*. Wiley, NY, 2001.